As per NEP 2020 Scheme Syllabus
w.e.f. Academic Year 2024-2025

UNIVERSITY of MUMBAI

First Year (F.E.) Degree Courses in Engineering
COMMON FOR ALL BRANCHES [Semester - II]

SEMICONDUCTOR PHYSICS

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A Text Book Of

SEMICONDUCTOR PHYSICS

For

Semester - II

(CODE : BSC2022)

F.E. DEGREE COURSES IN ENGINEERING
COMMON FOR ALL BRANCHES

AS PER NEP 2020 SCHEME SYLLABUS OF UNIVERSITY OF MUMBAI
W.E.F. ACADEMIC YEAR 2024-2025

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PREFACE

The physics research of today is the engineering of tomorrow! Physics leads science in the study of matter, energy and their interaction. Technology deals with innovative applications of scientific knowledge and engineering is concerned with the practical use of appropriate technologies.

Today the time taken between research breakthrough in physics and their applications to engineering has shrunk enormously. Technology is evolving at a rate faster than ever before. Hence it is necessary for engineering students to acquaint themselves with the frontier area of research in order to get conditioned for the atmosphere of change that they will encounter in their career.

This book is based on NEP syllabus of University of Mumbai. This book provides a basic understanding of Semiconductors in the field of Basic Engineering. The language of the book is kept simple and all topics are explained logically with examples and applications. Some of the topics are of highly demanding research areas and have been introduced for students to gain advanced knowledge upon entering the industry. Every chapter is enriched with solved problems, questions and practice problems.

I would like to express my deepest gratitude to Mr. Dinesh K. Furia, Mr. Pradeep K. Furia and Mr. Dhairya P. Furia of M/s Nirali Prakashan.

I am indeed thankful to Mr. Jayanth Dedhia for facilitating the coordination required for publishing this edition.

Suggestions are most welcomed for the revised edition.

Authors

SYLLABUS

Module I: Basics of Semiconductors — 4 Hrs.

Types of Semiconductors, Carrier Concentration in Intrinsic Semiconductors, Fermi Level of Intrinsic Semiconductors, Variation of Fermi Level of Intrinsic Semiconductors, wrt Temperature. Extrinsic Semiconductors, Fermi Level of Extrinsic Semiconductors, Variation of Fermi Level of Extrinsic Semiconductors, wrt Temperature and Impurity Concentration, Equation of Conductivity with Current Flow, Hall Effect, Calculation of Hall Voltage.

Module II: Junction Diode — 4 Hrs.

Formation of p-n Junction, Calculation of Barrier Potentials, Diode Equation, p-n Junction in Forward Bias, p-n Junction in Reverse Bias, Current- Voltage Curve for p-n Junction Diode, LED and its working.

Module III: Important Diodes — 4 Hrs.

Working of: Photo Diode, Solar Cell, Zenerdiode, Varactor Diode, Gunn Diode and their applications.

Module IV: Bipolar Junction Transistors — 4 Hrs.

BJT Structure and Operation - BJT Structure, Modes of Operation, CB, CE I-V Characteristics BJT Amplification and Switching - Current Gain, BJT as a Switch.

Module V: Field Effect Transistors — 6 Hrs.

Field-Effect Transistors (FETs) - FET Types: JFET, MOSFET, Structure and Operation MOSFETs in Detail - MOSFET Structure, Enhancement and Depletion Modes, Threshold Voltage MOSFET Applications - MOSFET as a Switch.

Module VI: Nano Technology — 4 Hrs.

Introduction to Nanotechnology, Properties (Optical, Electrical, Structural, Mechanical) Importance of Surface to Volume Ratio, Bonding in Solids (Vander Walls Interactions), Application: Lithography, Single Electron Transfer (SET), Spin Valves.

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Module - I

BASICS OF SEMICONDUCTORS

Syllabus:

- *Types of Semiconductors, Carrier concentration in intrinsic semiconductors, Fermi level of intrinsic semiconductors, Variation of fermi level of intrinsic semiconductors, with temperature. Extrinsic semiconductors, Fermi level of extrinsic semiconductors, Variation of fermi level of extrinsic semiconductors, with temperature and impurity concentration, Equation of conductivity with current flow, Hall effect, Calculation of hall voltage.*

Objectives:

- *To provide students with a basic understanding of semiconductors in the field of basic engineering.*

Outcome:

- *Learners will be able to Use and Demonstrate his/her ability earned here to apply it to calculate hall voltage.*

List of Contents:

1.1 *Band Theory of Solids*
1.2 *Fermi Dirac Distribution Functions*
1.3 *Density of States*
1.4 *Semiconductors and their Types*
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1.1 BAND THEORY OF SOLIDS

Band theory of solids is a theoretical model that explains the behavior of electrons (energy states of electrons) in solid materials. This theory is a fundamental concept in solid-state physics that explains the electrical, thermal, optical and insulative properties of materials. It provides the electronic levels in (ideal) crystal structures, which are characterized by two quantum numbers, the Bloch vector k and the band index n.

Here the Bloch vector is an element of the reciprocal space (in units 1/length) and the energy of the electron En(k) is a continuous function of k, so that one obtains a continuous range of energies referred to as the energy band. On this based we can illustrating how the atoms in a solid interacting to form bands of energy levels, which in turn influence the materials conductivity. Based on electrical conductivity, materials are divided into conductors, insulators and semiconductors. All dielectrics are insulators (non-conducting). Metals are good conductors of electricity.

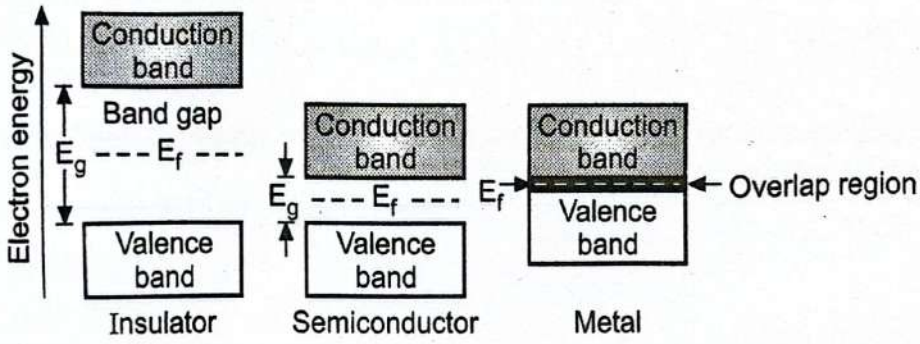


Fig. 1.1: Simplified diagram of band structure of insulators, semiconductors and metals

This theory has several key concepts that define the behavior of electrons in a solid.

- **Energy Bands:** When atoms form a solid, their closely spaced discrete energy levels merge into continuous bands. These bands are separated by energy gaps known as band gaps.
- **Band Gap:** The energy difference between the top of the valence band and the bottom of the conduction band. It is crucial in determining a material's electrical conductivity.
- **Valence Band:** The highest range of electron energies in which electrons are normally present at absolute zero temperature. It is filled with electrons in the ground state.
- **Conduction Band:** The band immediately above the valence band, which is partially filled with electrons or completely empty, allowing for electrical conductivity.

The available energies for electrons help us to differentiate between insulators, conductors and semiconductors. In free atoms, discrete energy levels are present, but in solid materials (such as insulators, semiconductors and conductors) the available energy states are so close to one another that they form bands.

Band gap is an energy range where no electronic states are present. In insulators, the valence band is separated from the conduction band by a large gap, in good conductors such as metals the valence band overlaps the conduction band, whereas in semiconductors there is a small gap between the valence and conduction bands, small enough to allow thermal excitation of electrons from the valence to conduction band. The overall representation in Fig. 1.1.

On the basis of conductivity, On the basis of the relative values of electrical conductivity (σ) or resistivity ($\rho = 1/\sigma$), the solids are broadly classified as:

1. **Conductors:** They have overlapping valence and conduction bands, allowing electrons to flow freely and conduct electricity efficiently. They possess very low resistivity (or high conductivity) example, metals. $\rho \sim 10^{-2} - 10^{-8} + \Omega$ m, $\sigma \sim 10^{2} - 10^{8}$ S m^{-1}.
2. **Semiconductors:** These materials have a small band gap that electrons can overcome at room temperature, making them partially conductive. They have resistivity or conductivity intermediate to metals and insulators. $\rho \sim 10^{-5} - 10^{6}\ \Omega$ m, $\sigma \sim 10^{5} - 10^{-6}$ S m^{-1}
3. **Insulators:** Characterized by a large band gap, insulators prevent electron flow, making them poor conductors of electricity. They have high resistivity. $\rho \sim 10^{11} - 10^{19}\ \Omega$ m, $\sigma \sim 10^{-11} - 10^{-19}$ S m^{-1}.

The values of ρ and σ given above are indicative of magnitude and could well go outside the ranges as well.

Materials Modification by Doping of Impurity

- **n-Type Semiconductors:** Created by adding donor atoms with extra electrons, which increase the number of free electrons in the conduction band.
- **p-Type Semiconductors:** Created by adding acceptor atoms with fewer electrons, creating "holes" in the valence band that act as positive charge carriers.

Applications of Band Theory

The versatility of band theory extends beyond just understanding the electrical properties of materials. It also plays a critical role in the development of optical devices and thermoelectric materials. For instance, the optical properties of materials, such as their ability to absorb, reflect, or transmit light, are dictated by the electronic transitions between different energy bands. This principle is exploited in photovoltaic cells and LED technology, where band theory guides the design of materials that efficiently convert light into electricity or vice versa.

Furthermore, band theory is instrumental in the study of thermoelectric materials, which convert temperature differences into electrical voltage and vice versa. By analyzing the band structure of these materials, we can optimize their efficiency for energy conversion, contributing to the development of sustainable energy technologies.

Advanced computational methods such as density functional theory (DFT), have enabled more precise predictions and analyses of band structures in complex materials. These computations help in designing new materials with tailored electronic properties for specific applications, pushing the boundaries of what is possible in electronics, photonics and energy technology.

1.2 FERMI DIRAC DISTRIBUTION FUNCTION

Definition: The Fermi Dirac distribution function describes the probability that a fermion, such as an electron, will occupy a particular energy level at a given temperature.

Fermi Dirac Distribution Expression

Mathematically, the probability of finding an electron in the energy state E at the temperature T is expressed as

$$f_{(E)} = \frac{1}{1 + \exp\left[\frac{(E - E_F)}{KT}\right]}$$

Where, K is the Boltzmann constant

T is the absolute temperature

Ef is the Fermi level or the Fermi energy

Role of Fermi Dirac Distribution Function

- The Fermi-Dirac distribution function is essential in electronics for understanding how many free electrons are available to conduct electricity in a material.
- The Fermi-Dirac distribution function is essential to explain the concentration of electrons in the conduction band.
- The Fermi-Dirac distribution function shows how electron energy states change with temperature, affecting the material's conductive properties.
- The Fermi-Dirac distribution function is useful for defining the position of the Fermi level.

Fermi Level: *It's an energy level where the probability of finding an electron is 50% with increase in temperature.*

The Fermi level is an important consequence of band theory, the highest occupied quantum state of electrons at absolute zero temperature. The position of the Fermi level relative to the conduction band is an important parameter that contributes to determining the electrical properties of a particular material. The position of the Fermi level is also indicated in Fig. 1.1.

The location of the Fermi energy is important, till all levels are occupied at zero K temperature. If the Fermi energy is located in a band gap, the material is insulating (or semiconducting) while it is metallic otherwise.

1.3 DENSITY OF STATES

The density of states (DOS) is a concept in solid-state physics that quantifies the number of available electron states at each energy level within a material. The **density of states** refers the number of different states at a particular energy level that electrons are allowed to occupy.

The density of states g(E) at an energy E is defined as the number of electronic states per unit energy per unit volume that are available to be occupied by electrons. In a crystalline solid, electrons occupy energy bands. It describes how these states are distributed within the bands. The band filled with electrons in the ground state termed as **Valence Band** and the band where electrons can move freely, contributing to electrical conductivity termed as **Conduction Band.**

In semiconductors, the density of states in the conduction band $g_c(E)$ and in the valence band $g_v(E)$ are important for determining electronic properties like carrier concentration and the conductivity. It is plotted as a function of energy. The resulting curve depends on the material's structure and electron interactions in it.

It is essential for understanding the electronic properties of materials, determining carrier concentrations and the energy distributions in materials including conductors, semiconductors and insulators. For a three-dimensional free electron gas, the density of states mathematically as:

$$g(E) = \frac{1}{2\pi^2}\left(\frac{2m}{\hbar^2}\right)^{3/2}\sqrt{E}$$

Where, m is the mass of the electron, $\hbar$ is the reduced Planck's constant and E is the energy.

Applications

- Useful for understanding the electronic properties of materials, such as conductivity, carrier concentration and Fermi level positioning.
- It is essential for calculating the number of electrons in the conduction and valence bands, particularly in semiconductors.
- Useful for studying the optical properties by determining how electrons absorb and emit photons.
- Useful for study of specific heat and thermal conductivity of materials especially at low temperatures.
- Understanding is required in designing and optimizing quantum devices like transistors, diodes and solar cells.

1.4 SEMICONDUCTORS AND THEIR TYPES

Semiconductors:

A semiconductor is a material that has a conductivity ranging between that of an insulator and a metal. Semiconductors have electrical conductivity that lies between metals and insulators. Good examples are silicon and germanium. They belong to the IV-A group. At 0 K, semiconductors behave like Insulators. At temperature greater than 0 K they behave like conductors. Pure germanium and silicon are called intrinsic semiconductors. By adding a small quantity of either group-III, group-V element atoms as impurities into pure Ge or Si, the electrical conductivity of these materials increases. This impure semiconductor is called an extrinsic semiconductors.

In many cases, their conducting properties may be altered in useful ways by introducing impurities (doping) in their based structure. When two differently doped regions exist in the same crystal, a semiconductor junction is created. The behavior of charge carriers, which include electrons, ions and electron holes, at these junctions is the basis of diodes, transistors and most modern electronics.

Some examples of semiconductors are silicon, germanium, gallium arsenide and elements near the so-called "metalloid staircase" on the periodic table. After silicon, gallium arsenide is the second-most common semiconductor and is used in laser diodes, solar cells, microwave-frequency integrated circuits and others. Silicon is a critical element for fabricating most electronic circuits.

Semiconductors are one of the technologically most important class of materials. It has a range of forbidden energies within the electronic structure of the material, known as the band gap. Semiconductors are used in manufactured of various kinds of electronic devices, including diodes, transistors and integrated circuits.

Other Properties of Semiconductors Include

1. The conductivity of semiconductors depends on its temperature and it is increased with increase in temperature.
2. The energy gap of a semiconductor decreases with rise in temperature.
3. At 0 K a semiconductor act like insulators.
4. The absence of an electron in the VB of a semiconductor is called hole. Hole occur only in the VB. Or an empty electron state is called a hole.
5. Like electrons, the hole in the VB also conduct electricity in case of a semiconductor.
6. The electric current in a semiconductor is the sum of the currents due to electron and hole.
7. Hole is a positive charge carrier of current.
8. They can be modified by doping to make semiconductor devices suitable for energy conversion, switches and amplifiers.
9. They have lesser power losses. They are smaller in size and possess less weight.
10. Their resistivity is higher than conductors but lesser than insulators.

Types of Semiconductors

1. On the basis of transition from valence band to conduction band, it classified as: (a) Indirect Band Gap Semiconductor and (b) Direct Band Gap Semiconductor

2. On the basis of relative concentration of holes and electrons, it classified as (a) Intrinsic Semiconductor and (b) Extrinsic semiconductor.

1.4.1 Intrinsic Semiconductors

An intrinsic semiconductor is a pure semiconductor having no impurities. In this semiconductor, the numbers of excited electrons and holes are equal, i.e., n = p as shown in Fig. (1.4 a). The semiconductor that is pure and has the number of electrons in the CB equal to the number of holes in the VB is called an intrinsic semiconductor. The examples of intrinsic semiconductors are pure silicon and pure germanium.

As we know, Si and Ge have four valence electrons. In its crystalline structure, every Si or Ge atom tends to a share one of its four valence electrons with each of its four nearest neighbour atoms and also to take share of one electron from each such neighbor.

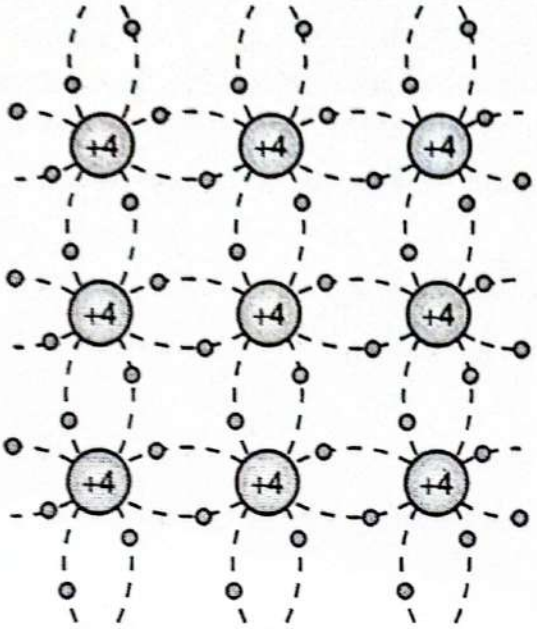


Fig. 1.2: Intrinsic semiconductor

In intrinsic semiconductors, the number of free electrons, ne is equal to the number of holes 'nh'. That is $n_e = n_h = n_i$

Where, n_i is called intrinsic carrier concentration.

1.4.2 Extrinsic Semiconductors

The conductivity of an intrinsic semiconductor depends on its temperature, but at room temperature its conductivity is very low. As such, no important electronic devices can be developed using these semiconductors. Hence there is a necessity of improving their conductivity. This can be done by making use of impurities in it. When a small amount, say, a few parts per million (ppm), of a suitable impurity is added to the pure semiconductor, the conductivity of the semiconductor is increased manifold. Such materials are known as extrinsic semiconductors or impurity semiconductors.

Definition: A semiconductor in which doping has been introduced or deliberate addition of a desirable impurity, thus changing the relative number and type of free charge carriers, is called as doped or extrinsic semiconductor. Impurity atoms are called dopants.

The dopant has to be such that it does not distort the original pure semiconductor lattice. It occupies only a very few of the original semiconductor atom sites in the crystal. A necessary condition to attain this is that the sizes of the dopant and the semiconductor atoms should be nearly the same.

There are two types of dopants used in pure semiconductors as

(i) Pentavalent (valency 5); like Arsenic (As), Antimony (Sb), Phosphorous (P), etc

(ii) Trivalent (valency 3); like Indium (In), Boron (B), Aluminium (Al), etc.

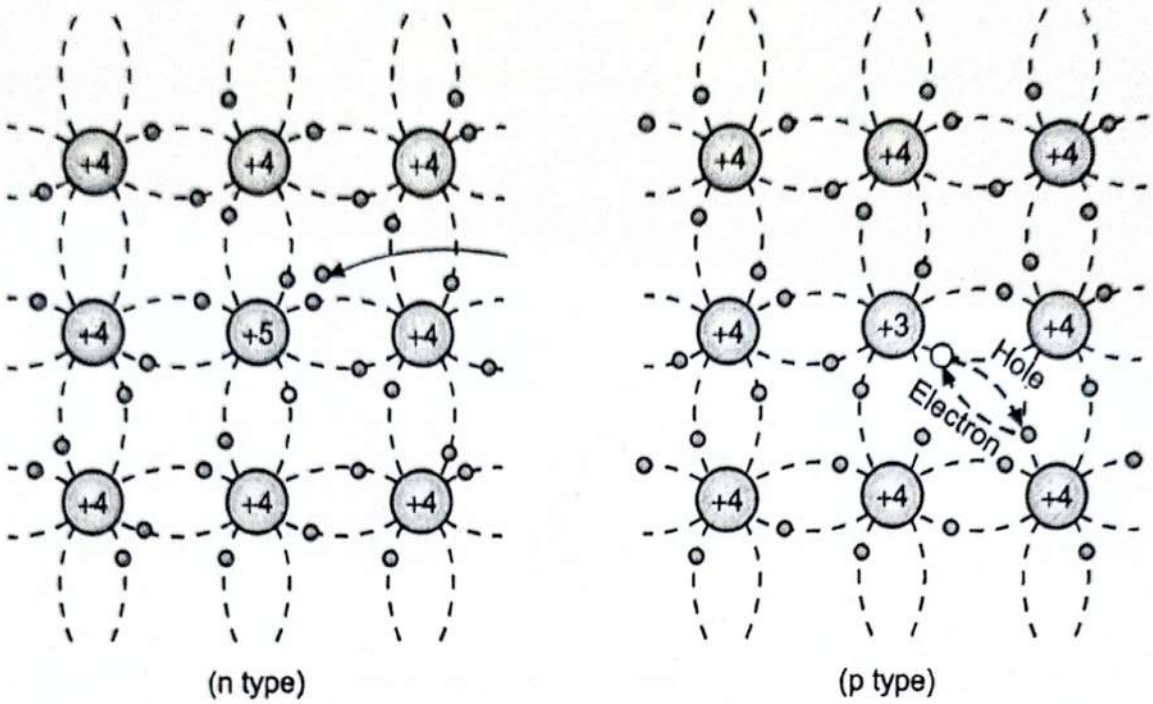


Fig. 1.3: Extrinsic semiconductor

An extrinsic semiconductor, in which conduction electrons are the majority carriers is an n-type semiconductor and its band diagram is illustrated in Fig. (1.4 b); one in which the holes are the majority charge carriers is a p-type semiconductor and is indicated in Fig. (1.4 c).

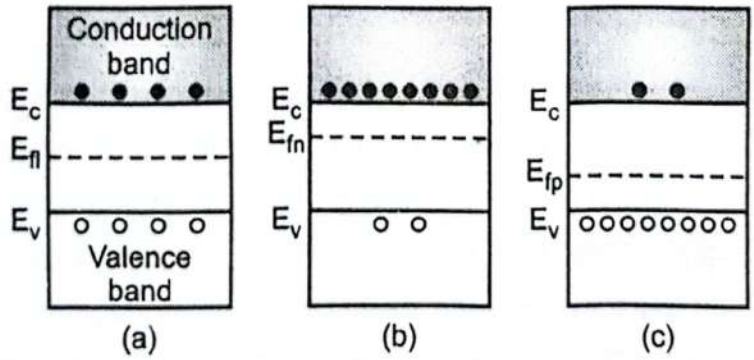


Fig. 1.4: Energy band diagrams for (a) intrinsic semiconductor, (b) extrinsic semiconductor (n-type), (c) extrinsic semiconductor (p-type). E_f is the Fermi energy level and letters i, n and p indicate intrinsic, n and p-type materials. E_c and E_v are the edges of conduction and valence bands

In a doped semiconductor the total number of conduction electrons n_e is due to the electrons contributed by donors and those generated intrinsically, while the total number of holes n_h is only due to the holes from the intrinsic source. But the rate of recombination of holes would increase due to the increase in the number of electrons. As a result, the number of holes would get reduced further. Thus, with the proper level of doping the number of conduction electrons can be made much larger than the number of holes. Hence in an extrinsic semiconductor doped with pentavalent impurity, electrons become the majority carriers and holes the minority carriers. These semiconductors are, therefore, known as n-type semiconductors.

For n-type semiconductors, $n_e >> n_h$

It is obvious that one acceptor atom gives one hole. These holes are in addition to the intrinsically generated holes, while the source of conduction electrons is only intrinsic generation.

Thus, for such a material, the holes are the majority carriers and electrons are minority carriers. Therefore, extrinsic semiconductors doped with trivalent impurity are called p-type semiconductors. For p-type semiconductors, the recombination process will reduce the number (n_i) of intrinsically generated electrons to n_e.

For p-type semiconductors $n_h >> n_e$

At room temperature, most of the acceptor atoms get ionized leaving holes in the valence band. Thus at room temperature the density of holes in the valence band is predominantly due to impurities in the extrinsic semiconductor.

The electron and hole concentration in thermal equilibrium in a semiconductor is as,

$$n_e n_h = n_i^2$$

1.5 CARRIER CONCENTRATION IN INTRINSIC SEMICONDUCTORS

Carrier Concentration (n_i)

Definition: The number of free electrons and holes per unit volume of the intrinsic semiconductor is called intrinsic carrier concentration (n_i) and remains constant.

i.e., $np = (n_i)(n_i)$

$$np = n_i^2$$

Electron Concentration:

Definition: The number of free electrons per unit volume of the conduction band of a given intrinsic semiconductor is called electron concentration, represented by 'n'.

Hole Concentration:

Definition: The number of holes per unit volume of the valence band of a given intrinsic semiconductor is called hole concentration, represented by 'p'.

Let the number of free electrons per unit volume of semiconductor having energies E and E + dE in CB be represented by n (E) dE. It is obtained by multiplying the density of energy states ZC (E) d (E). [Number of energy states per unit volume] and Fermi Dirac distribution function for the Probability of occupation of electrons FC (E).

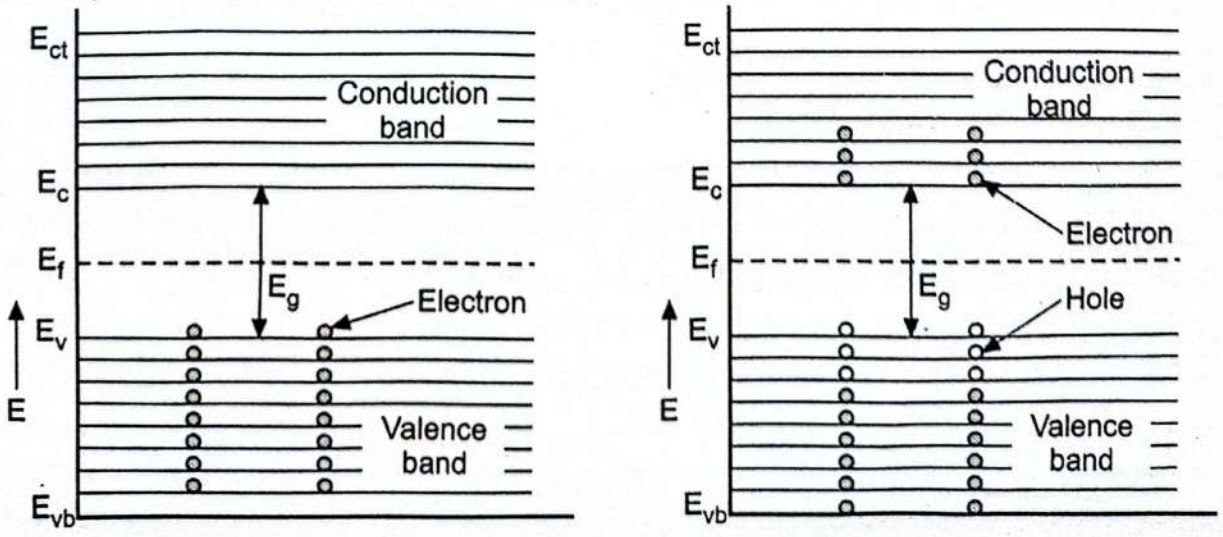


Fig. 1.5

The constant product of electron and hole concentration is $n_i^2 = (n\ p)$

Density of electron is,

$$n = N_c\, e^{(Ef-Ec)/kT}$$

Density of hole is,

$$p = N_v\, e^{(Ev-Ef)/kT}$$

We know, $N_c = 2(2\pi m_e kT/h^2)^{3/2}$

and $N_v = 2(2\pi m_p kT/h^2)^{3/2}$

Where, m_e and m_p are the effective mass of electron and hole respectively.

Therefore, $n_i^2 = N_c\, e^{(Ef-Ec)/kT}\, N_v\, e^{(Ev-Ef)/kT}$

$$n_i^2 = N_c N_v\, e^{(-Ec+Ev)/kT}$$

$$n_i^2 = N_c N_v\, e^{-(Ec-Ev)/kT}$$

$$\mathbf{n_i^2 = N_c N_v\, e^{-(Eg)/kT}}$$

Therefore, $\mathbf{n_i = \sqrt{N_c N_v\, e^{-(Eg)/2kT}}}$

1.6 FERMI LEVEL OF INTRINSIC SEMICONDUCTORS

At any temperature T > 0 k in an intrinsic semiconductor, a number of electrons are found in the conduction band and the rest of the valence electrons are left behind in the valence band.

The total number of electrons in the intrinsic semiconductor is

$$N = n_c + n_v \qquad \text{...(1)}$$

Where, n_c = number of electrons in conduction band

n_v = number of electrons in valence band

The probability of occupancy of an energy level in the conduction band can be written as

$$F_{(E_c)} = \frac{1}{1 + e^{[(E_c - E_F)/kT]}}$$

Where, E_c is the minimum energy required for the electron to reach the bottom level of conduction band. Hence, the number of electrons found in the conduction band is

$$n_e = Nf_{(E_c)} = \frac{N}{1 + e^{[(E_c - E_F)/kT]}} \qquad \text{... (2)}$$

Similarly, n_v is the number of valence electrons left behind in the valence band from the total N electrons.

The probability of occupancy of a level in valence band is

$$F_{(E_v)} = \frac{1}{1 + e^{-(E_F - E_v)/kT}}$$

Hence, the number of electrons in the valence band can be written as

$$n_v = NF_{E_v} = \frac{N}{1 + e^{-(E_F - E_v)/kT]}} \qquad \text{... (3)}$$

Substituting (2) and (3) in (1), we have

$$N = \frac{N}{1 + e^{(E_c - E_F)/kT}} + \frac{N}{1 + e^{-(E_F - E_V)/kT}}$$

$$\therefore \quad 1 = \frac{1}{1 + e^{(E_c - E_F)/kT}} + \frac{1}{1 + e^{-(E_F - E_V)/kT}}$$

$$1 = \frac{2 + e^{-(E_F - E_V)/kT} + e^{(E_c - E_F)/kT}}{[1 + e^{(E_c - E_F)/kT}]\,[1 + e^{-(E_F - E_V)/kT}]}$$

After solving this we get as below,

$$e^{(E_c - 2E_F + E_V/kT} = 1 \qquad \{e^0 = 1\}$$

$$E_c + E_v - 2E_F = 0$$

$$E_c + E_v = 2E_F$$

$$\therefore \quad \mathbf{E_F = \frac{E_c + E_v}{2}}$$

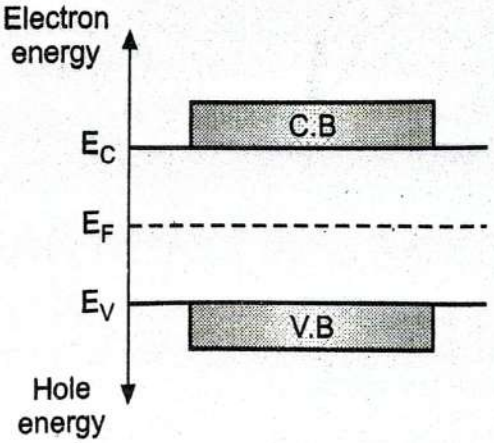


Fig. 1.6: Position of fermi level in intrinsic semiconductor

Thus, the Fermi level lies in the middle of the forbidden energy gap of an intrinsic semiconductor as shown Fig. 1.6. As the temperature increases, the electrons move from VB to CB. Also the Fermi level slightly rises upwards towards CB.

1.7 VARIATION OF FERMI LEVEL OF INTRINSIC SEMICONDUCTOR WITH TEMPERATURE

In an n-type semiconductor, the electron concentration dependence is shown in Fig. 1.7. At 0 k, the donor atoms are not ionized i.e., all donor electrons are bound to donor atoms. Thus, the conduction band is empty and the valence band is full. As a result, the material behaves as an insulator.

As the temperature increases, donor atoms are ionized and the donor electrons go into the conduction band, but holes are not produced in the valence band.

At about 100 k, the donor levels are all ionized further increases in temperature do not produce electrons and the curve levels off. The plateau region is called the **depletion region**.

As the temperature increases further, some electrons from the valence band are also excited into the conduction band leaving behind holes in the valence band.

At very high temperature, the intrinsic behavior takes over as large number of electron in the valence band gets excited to the conduction band exceeding the number of donor electrons.

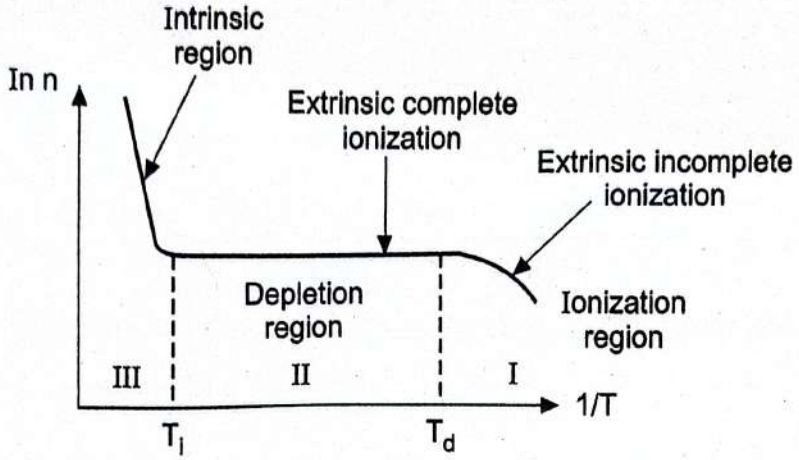


Fig. 1.7: Electron concentration with increase in temperature

1.8 CARRIER CONCENTRATION IN EXTRINSIC SEMICONDUCTORS

Charge Densities in p-Type and n-Type Semiconductor:

Mass Action Law:

Under thermal equilibrium for any semiconductor, the product of the number of holes and the concentration of electrons is constant and is independent of amount of donor and acceptor impurity doping.

$$n.p = n_i^2$$

Where n = electron concentration,

p = hole concentration,

n_i^2 = intrinsic concentration

Hence in an N-type semiconductor, as the number of electrons increase the number of holes decreases. Similarly in P-type as the number of holes increases, the number of electrons decreases. Thus the product is constant and is equal to n^2 in the case of intrinsic as well as extrinsic semiconductors.

The law of mass action has given the relationship between free electron concentration and hole concentration. These concentrations are further related by the law of electrical neutrality as explained below.

Law of Electrical Neutrality:

Semiconductor materials are electrically neutral. According to the law of electrical neutrality, in an electrically neutral material, the magnitude of positive charge concentration is equal to that of negative charge concentration. Let us consider a semiconductor that has ND donor atoms per cubic centimeter and NA acceptor atoms per cubic centimeter i.e., the concentration of donor and acceptor atoms are ND and NA respectively. Therefore, ND positively charged ions per cubic centimeter are contributed by donor atoms and NA negatively charged ions per cubic centimeter are contributed by the acceptor atoms.

Let n, p is concentration of free electrons and holes respectively. Then according to the law of neutrality

$$ND + p = NA + n$$

For N-type semiconductor,

$$NA = 0 \text{ and } n >> p.$$

Therefore, $\mathbf{N_D \approx n}$

Hence, for N-type semiconductor free electron concentration is approximately equal to concentration of donor atoms.

Therefore, current density in N-type semiconductor is

$$J = N_D \mu_n q E$$

And conductivity,

$$\sigma = N_D \mu_n q$$

For P-type semiconductor,

$$ND = 0 \quad \text{and} \quad p >> n$$

Therefore, $\mathbf{N_A \approx p}$

Hence for P-type semiconductor hole concentration is approximately equal to concentration of acceptor atoms.

Therefore, current density in P-type semiconductor is

$$J = N_A \mu_p q E$$

And conductivity,

$$\sigma = NA \mu_p q$$

Mass Action Law for N-Type:

$$pn = n_i^2$$

$$p = n_i^2/N_D, \text{ since } (n \approx N_D)$$

Mass Action Law for P-Type:

$$pn = n_i^2$$

$$n = n_i^2/N_A \text{ since } (p \approx N_A)$$

Charge Densities in Semiconductor:

The electron density in N-type is,

$$n = \sqrt{(N_e N_d)\, e^{-(Ec-Ed)/2kT}}$$

The hole density in P-type is,

$$p = \sqrt{(N_a N_h)\, e^{-(Ea-Ev)/2Kt}}$$

Where,

$$N_h = 2(2\pi m_e kT/h^2) \text{ and } N_d = 2(2\pi m_p kT/h^2)$$

1.9 FERMI LEVEL OF EXTRINSIC SEMICONDUCTORS

A semiconductor doped with an impurity atom (**dopant**) is termed as **extrinsic semiconductor**. It has two types: n-type and p-type semiconductors.

1. **Fermi Level in n-Type Semiconductor:** At normal temperature, the donor atoms cannot interact with each other and their energy levels are discrete levels E_D. They are called donor level. In an n-type semiconductor, the donor level is just below the bottom of the conduction band. The number of electrons is more. So, the Fermi level shifts from intrinsic level E_{Fi} to E_{Fn} shown in Fig. 1.8.

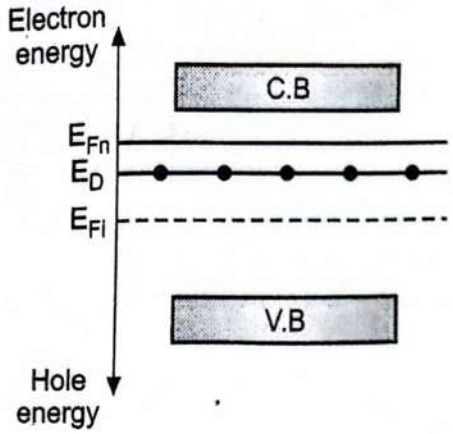


Fig. 1.8: Position of fermi level in n-type semiconductor

2. **Fermi Level in p-Type Semiconductor:** In p-type semiconductors at an ordinary temperature, the number of holes is much greater than the number of electrons. Hence, the Fermi level shifts from E_{Fi} to E_{Fp} towards the valence band, as shown in Fig. 1.9.

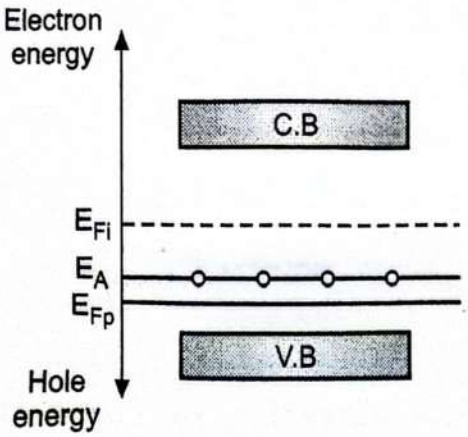


Fig. 1.9: Position of fermi level in p-type semiconductor

1.10 VARIATION OF FERMI LEVEL OF EXTRINSIC SEMICONDUCTORS WITH TEMPERATURE

1. In n-Type Semiconductor

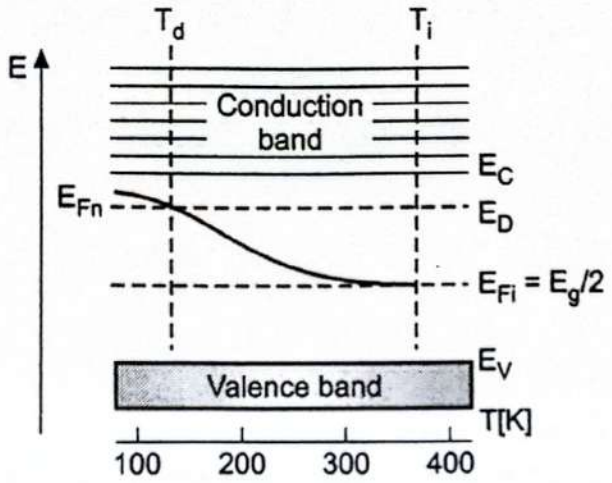


Fig. 1.10: Effect of temperature in n-type semiconductor

2. In p-Type Semiconductor

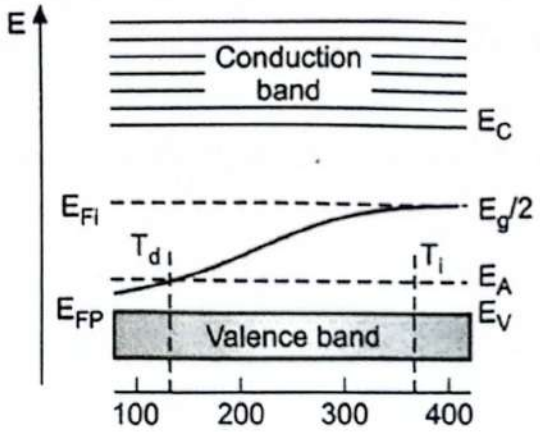


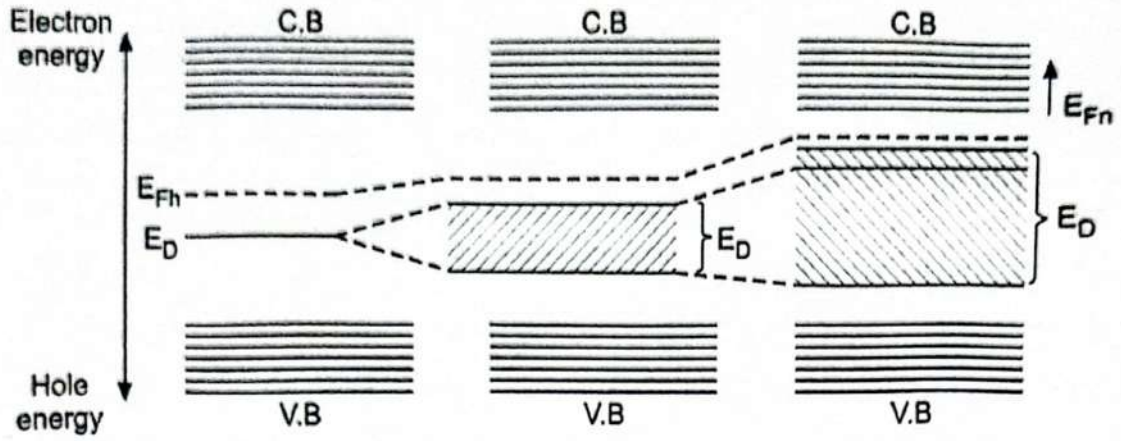
Fig. 1.11: Effect of temperature in p-type semiconductor

1.11 VARIATION OF FERMI LEVEL OF EXTRINSIC SEMICONDUCTORS WITH IMPURITY CONCENTRATION

(i) In n-Type Semiconductor: At low impurity concentrations, the impurity atoms are distantly spaced from one another. Therefore, they do not interact with increase in impurity concentration. As the spacing between them decreases, they interact with splitting in donor levels and form an energy band below the conduction band as shown in Fig. 1.12.

The larger the doping concentration, the broader the impurity band and a stage comes when the impurity band overlaps the conduction band, as a result there is a decrease in width of the forbidden gap. Thus, the Fermi level displaces upwards.

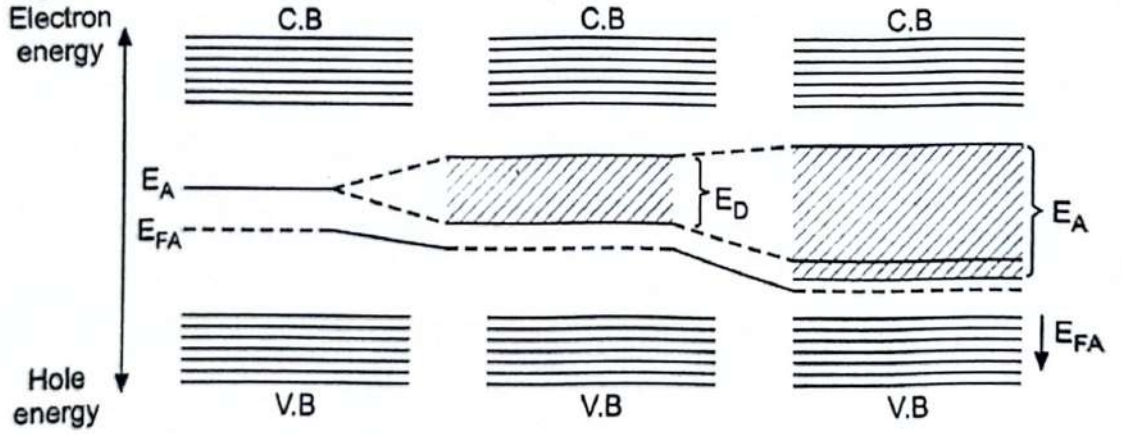
The Fermi level shifts closer and closer to the conduction band with an increase in impurity conduction and finally moves into the conduction band when the donor band overlaps the conduction band.



(a) Low doping level (b) Medium doping level (c) High doping level

Fig. 1.12: Effect of concentration on fermi level in n-type semiconductor

(ii) In p-Type Semiconductor: In a p-type semiconductor, with increase in doping concentration, the acceptor level broadens into a band. Finally, it overlaps the valence band. *The Fermi level moves closer to the valence band and finally at very high impurity concentration,* it will shift into the valence band. Here also the E_g reduces which is the foundation of band gap engineering.



(a) Low doping level (b) Medium doping level (c) High doping level

Fig. 1.13: Effect of concentration on fermi level in p-type semiconductor

Conductivity in Semiconductors:

In a pure (intrinsic) semiconductor, the number of holes is equal to the number of electrons. Thermal agitation continues to produce new electron-hole pairs and the electron hole pairs disappear because of recombination. With each electron hole pair created, two charge carrying particles are formed. One is negative which a free electron with mobility μ_n. The other is a positive i.e., hole with mobility μ_p. The electrons and holes move in opposite directions in an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic semiconductor is given by

$$\begin{aligned} J &= J_n + J_p \\ &= q\,n\,\mu_n\,E + q\,p\,\mu_p\,E \\ &= (n\,\mu_n + p\,\mu_p)\,qE \\ &= \sigma E \end{aligned}$$

Where, n = number of electrons / unit volume i.e., concentration of free electrons

p = number of holes / unit volume i.e., concentration of holes

E = applied electric field strength, V/m

q = charge of electron or hole in Coulombs

σ is the conductivity of semiconductor which is equal to $(n \mu_n + p \mu_p) q$.

The resistivity of a semiconductor is the reciprocal of its conductivity. It is evident from the above equation that current density in a semiconductor is directly proportional to applied electric field E.

For pure semiconductor, $n = p = n_i$

Where n_i = intrinsic concentration,

The value of n_i is given by

$$n^2 = AT3 \exp(-E/KT)$$

Therefore, $J = n_i (\mu_n + \mu_p) q E$

Hence conductivity in intrinsic semiconductor is

$$\sigma = n_i (\mu_n + \mu_p) q$$

Conductivity in Extrinsic Semiconductor (N-Type and P-Type):

The conductivity of intrinsic sc is given by $\sigma = n_i (\mu_n + \mu_p) q = (n \mu_n + p \mu_p)q$

For N-type, n>>p, Therefore $\sigma = q n \mu_n$

For P-type, p>>n, Therefore $\sigma = q p \mu_p$

1.12 EQUATION OF CONDUCTIVITY WITH CURRENT FLOW

Conductivity (σ) is to measure the ability of materials to conduct electric current in it. It's a reciprocal of resistivity (ρ). The relationship between electric current (I), conductivity (σ), electric field (E) and the cross-sectional area of the conductor (A) can be described using Ohm's law in its differential form and the formula for current density (J).

Ohm's Law (Differential Form)

$$J = \sigma E$$

J is the current density (current per unit area), measured in amperes per square meter (A/m^2).

σ is the electrical conductivity, measured in Siemens per meter (S/m).

E is the electric field, measured in volts per meter (V/m).

Relationship between Current Density and Current

The current density of J is related to the electric current I and the cross-sectional area A through the following equation:

$$I = J A$$

Combining these equations.

Equation for Electric Current with Conductivity

$$I = \sigma E A$$

Where, I is the electric current, measured in amperes (A), σ is the conductivity measured in Siemens per meter (S/m), E is the electric field, measured in volts per meter (V/m) and A is the cross-sectional area of the conductor, measured in square meters (m^2).

These equations illustrate how conductivity is directly related to the electric current flow in a material. Higher conductivity means lower resistance to the flow of electric current, allowing more current to pass through the material for a given electric field.

1.13 HALL EFFECT AND CALCULATION OF HALL VOLTAGE

Principle of Hall Effect:

If a conductor or semiconductor carrying a current I is placed in a transverse magnetic field B, an electric field E is induced in the direction perpendicular to both I and B. This phenomenon is known as **Hall Effect** and the electric field or voltage induced termed as **Hall voltage** (V_H).

Experimental determination of V_H. Consider the specimen where current is flowing in the positive x-direction and the magnetic field is in the positive z-direction. The force exerted on charge carriers, the electrons, is downwards. Thus, a voltage called Hall voltage is developed with positive at the upper surface and negative at the lower surface. Thus, hall voltage to be calculated refers to Fig. 1.14.

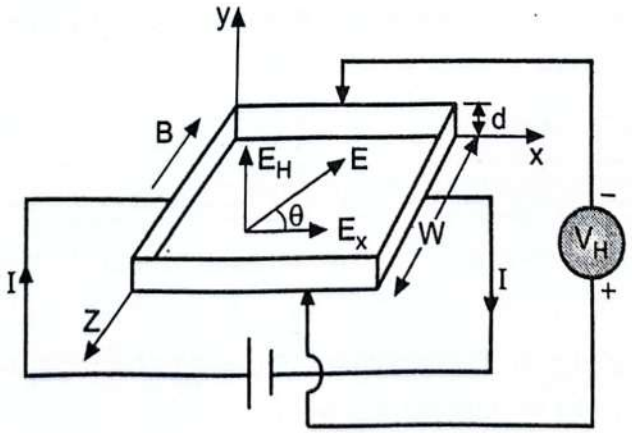


Fig. 1.14: Hall Experimental set up

Assume n-type or p-type Semiconductor, then magnetic force is experienced by electrons towards the y direction, as it is applied transversely.

∴ Magnetic force,

$$F = Be\upsilon$$

Holes also experience a force but in the positive y direction, thus creating a potential difference between both the surfaces denoted by V_H called Hall voltage.

$$\therefore \quad E_H = \frac{V_H}{w} \qquad \ldots (1)$$

The current flowing through it is given by,

$$\mathbf{I = nAe\upsilon} \qquad \ldots (2)$$

Force experienced due to electric field is given by

$$F = eE_H$$

In equilibrium condition, the force due to electric field and force due to magnetic field balances to each other.

$$\therefore \quad eE_H = Be\upsilon$$

$$E_H = B\upsilon \quad \ldots (3)$$

$$\frac{V_H}{W} = B\upsilon \quad \ldots \text{Using equation (1)}$$

$$\therefore \quad V_H = B\upsilon w \quad \ldots (4)$$

From eq. (2) $\quad \upsilon = \frac{I}{neA} = \frac{J}{ne} \quad \left\{J = \frac{I}{A}\right\}$

$\therefore$ From eq. (4)

$$V_H = \frac{IBw}{neA} = \frac{BwJ}{ne}$$

As $\quad A = w \times d,$

where, $\quad w =$ width,

$d =$ depth,

$A =$ area of specimen

$$V_H = \frac{IB}{ned} \quad \text{Or} \quad V_H = \frac{R_H IB}{d}$$

V_H can calculate by using values of I, B, d, n and e or R_H,

Hall coefficient is Hall field per unit current density per unit magnetic induction

$$R_H = \frac{E_H}{JB} = \frac{\frac{V_H}{w}}{JB} = \frac{\frac{BJ}{ne}}{JB} = \frac{1}{en_e}$$

$$V_H = \frac{R_H IB}{d}$$

$$R_H = \frac{1}{en} \text{ (p-type semiconductor) and}$$

$$R_H = -\frac{1}{en_e} \text{ (n-type semiconductor)}$$

As $\quad \sigma = \mu n_e \quad \boxed{\mu = \frac{\sigma}{n_e} = \sigma R_H}$

Therefore, if conductivity and Hall coefficient are measured, the mobility and density of carriers can be determined. It is noted that in semiconductors, carrier concentration increases with an increase in temperature hall coefficient decreases. The unit of R_H is m^3/C.

The net electric field E acting on the charge carrier is a constant of applied electric field E_x and Hall electric field E_H. The angle made by E with the x-axis is called the Hall angle, given by $\theta_H = \tan^{-1}\left(\frac{E_H}{E_x}\right)$ or $\theta_H = \tan^{-1}(R_H \sigma B)$.

Applications

- The hall Effect is useful for finding the following characteristics in a metal o semiconductor.
- The type of charge carrier.
- The charge carrier concentration.
- If the conductivity of the material is known, the mobility of charge carriers can b calculated.
- The mean drift velocity of the majority charge carrier.
- Measurement of magnetic field, as Hall voltage is proportional to the magnetic fiel intensity for a given current in a sample.

Other Applications: A Hall Effect sensor is a transducer that produces its output voltage i response to changes in magnetic field. Hall sensors can be used to measure heavy current withou interrupting the circuit. E.g., proximity switching, positioning speed detection and current sensin applications.

1.14 NUMERICALS

Problem 1.1: *The Fermi level of potassium is 2.1 eV. Calculate the velocity of the electron at the Fermi level.*

Solution: Formula: $E_F = \frac{1}{2} m v_F^2$

$$v_F^2 = \frac{2E_F}{m} = \frac{2.2 \times 1 \times 1.602 \times 10^{-19}}{9.1 \times 10^{-31}} = 0.74 \times 10^{12}\ m^2/s^2$$

$$v_F = 8.6 \times 10^5\ m/s$$

$$v_F = \mathbf{8.6 \times 10^5\ m/s}$$

Problem 1.2: *In a solid, consider the energy level lying 0.01 eV below Fermi level. What is the probability of this level not being occupied by an electron?*

Solution: Formula:

$$(E_F - E) = [E_F - (E_F - 0.01) = 0.01\ eV$$

$$kT = 0.026\ eV \text{ (known) at } T = 300\ K$$

The probability of energy level E not being occupied by an electron is given by $[1 - F_{(E)}]$.

$$[1 - F_{(E)}] = 1 - \frac{1}{1 + e^{(E - E_F)/kT}} = \frac{1}{1 + e^{(E_F - E)/kT}}$$

$$= \frac{1}{1 + e^{0.01\ eV/0.026\ eV}} = \frac{1}{1 + e^{0.385}} = \frac{1}{1 + 1.47} = \mathbf{0.405}$$

Probability is 0.405.

Problem 1.3: *Find the temperature at which there is 1% probability that a state with energy 2 eV is occupied. Given that Fermi energy is 1.5 eV.*

Solution: Formula:

$$F_{(E)} = \frac{1}{1 + \exp^{[(E - E_F)/kT]}}$$

$$E - E_F = 2 \text{ eV} - 1.5 \text{ eV} = 0.5 \text{ eV}$$

$$F_{(E)} = 1\%$$

$$\therefore \quad \frac{1}{100} = \frac{1}{1 + \exp^{0.5/kT}}$$

$$e^{0.5/kT} = \frac{0.99}{0.01} = 99$$

Taking log on both sides $\frac{0.5}{kT} = 2.303 \log 99$

$$T = \frac{0.5 \text{ eV}}{2.303 \log 99 \times 8.61 \times 10^{-5} \text{ eV}} = 1262 \text{ K}$$

$$T = \mathbf{1262\ K}$$

Hall Effect

Problem 1.4: *The resistivity of Cu is 1.72 $\times 10^{-8}$ ohm-m. Calculate the mobility of electrons in Cu. Given that: Number of electrons per unit volume is 10.41 $\times 10^{28}/m^3$.*

Solution: Given: Resistivity of Cu (ρ) = 1.72×10^{-8} ohm-m

Number of electrons per unit volume (n) = $10.41 \times 10^{28}/m^3$

Formula:

$$\sigma = \frac{1}{\rho} = \frac{1}{1.72 \times 10^{-8}} = 58.13 \times 10^6 \text{ mho per meter}$$

$$\sigma = ne\mu_e$$

$$\mu_e = \frac{\sigma}{ne} = \frac{58.13 \times 10^6}{10.41 \times 10^{28} \times 1.6 \times 10^{-19}}$$

$$\mu_e = \mathbf{3.49 \times 10^{-3}\ m^2/volt\text{-}sec}$$

Problem 1.5: *The mobility of holes is 0.025 m^2/volts sec. What would be the resistivity of a p-type silicon, if the Hall co-efficient of sample is 2.25 $\times 10^{-5}$ m^3/c?*

Solution: Given: Mobility of holes (μ_h) = 0.025 m^2/volts-sec.

Hall co-efficient (R_H) = 2.25×10^{-5} m^3/c.

Formula: Conductivity of p-type semiconductor

$$\sigma_p = \rho\, e\mu_n \qquad R_H = \frac{1}{pe}$$

$$\sigma_p = \frac{\mu h}{R_H} = \frac{0.025}{2.25 \times 10^{-5}} = 1111.11 \text{ mho per meter}$$

$$\text{Resistivity } (\rho) = \frac{1}{\sigma} = \frac{1}{1111.11} = \mathbf{9.00 \times 10^{-4}\ ohm\ meter}$$

Problem 1.6: *Find resistivity of intrinsic germanium at 300 k. Given density of carriers is $2.5 \times 10^{19}/m^3$. Mobility of electrons is 0.39 m^2/volt-sec and mobility of holes is 0.19 m^2/v-sec charge of electron is 1.6×10^{-19} c.*

Solution: Given: Mobility of electrons (μ_e) = 0.39 m^2/volts-sec.

Mobility of holes (μ_h) = 0.19 m^2/volts-sec.

Density of carriers (n) = $2.5 \times 10^{19}/m^3$.

Charge of electron (e) = 1.6×10^{-19} c

Formula: Conductivity of intrinsic germanium is given by σ.

$$\sigma_{total} = \sigma_n + \sigma_p = (ne\mu_n) + (ne\mu_h)$$

In case of intrinsic semiconductor, $n = p = 2.5 \times 10^{19}/m^3$

$$\sigma_{total} = [ne(\mu_n + \mu_h)] = [2.5 \times 10^{19} \times 1.6 \times 10^{-19} (0.39 + 0.19)]$$

$$\sigma_{total} = 2.32 \text{ mho/meter}$$

$\therefore$ Resistivity of intrinsic germanium (ρ),

$$\rho = \frac{1}{\sigma} = \frac{1}{2.32} = 0.43$$

$$\rho = \mathbf{0.43 \text{ ohm-meter}}$$

Problem 1.7: *In intrinsic Ge, the carrier concentration is $2.5 \times 10^{19}/m^3$. The electron and hole mobilities are 0.39 m^2/v-sec and 0.17 m^2/v-sec respectively. Find the resistance of a Ge rod of 2 cm × 1 mm × 1 mm dimension.*

Solution: Given: $n_i = 2.5 \times 10^{19}/m^3$, $\mu_e = 0.39$ m^2/v-sec, $\mu_h = 0.17$ m^2/v-sec

A = 1 sq.mm = 10^{-6} mm^2, l = 2 cm = 2×10^{-2} m

Formula:

$$\rho = \frac{1}{\sigma}$$

$$\sigma = n_i (\mu_e + \mu_h) e$$

$$\sigma = 2.5 \times 10^{19} (0.39 + 0.17) \times 1.6 \times 10^{-19} = 2.24 \text{ mho/m}$$

$$\rho = \frac{1}{\sigma} = \frac{1}{2.24} = 0.4464 \ \Omega \text{ m}$$

$$R = \rho \frac{l}{A} = 0.4464 \times \frac{2 \times 10^{-2}}{10^{-6}} = \mathbf{8.92 \times 10^3 \ \Omega}$$

Problem 1.8: *A sample of n-type silicon has a doner density of $10^{20}/m^3$. It is used in the Hall Effect experiment. If the sample of width 4.5 mm is kept in a magnetic field of (0.55T) with current density of 500 A/m^2, find: (1) Hall voltage developed in it. (2) Hall coefficient. (3) Hall angle of mobility of electrons is 0.17 m^2/V sec.*

Solution: Given: Doner density $N_D = 10^{20}/m^3$, Width (w) = 4.5 mm = 4.5×10^{-3} m

Magnetic field (B) = 0.55 Tesla, Current density (J) = 500 A/m^2

Mobility of electron (μ_e) = 0.17 m^2/V sec

Formula: (1) Hall voltage,

$$V_H = \frac{JBw}{ne}$$

Put $n = N_D$,

$$V_H = \frac{500 \times 0.55 \times 4.5 \times 10^{-3}}{10^{20} \times 1.6 \times 10^{-19}}$$

$$= \mathbf{0.0773\ volts}$$

(2) Hall coefficient (R_H)

$$R_H = \frac{1}{ne} = \frac{1}{NDe} = \frac{1}{10^{20} \times 1.6 \times 10^{-19}}$$

$$= \mathbf{0.0625\ m^3/c}$$

(3) Hall angle

$$\tan\theta = \mu_e B = 0.17 \times 0.55$$

$$\tan\theta = 0.0935$$

$$\theta = \mathbf{5.31°}$$

Problem 1.9: *The Hall coefficient of a specimen of a doped silicon is found to be 3.66×10^{-4} m^3/c. The resistivity of the specimen is 8.93×10^{-3} Ω-m. Find the mobility and density of the charge carrier.*

Solution: Given: Hall coefficient (R_H) = 3.66×10^{-4} m^3/c

$\rho = 8.93 \times 10^{-3}\ \Omega$ m, μ = ?, n = ?

Formula: (1) Hall coefficient (R_H)

$$R_H = \mathbf{\frac{1}{ne}}$$

$$n = \frac{1}{R_H e} = \frac{1}{3.66 \times 10^{-4} \times 1.6 \times 10^{-19}} = 1.707 \times 10^{22}/m^3$$

(2) Mobility of the charge carrier, $\boldsymbol{\sigma = ne\mu}$

$$\mu = \frac{\sigma}{ne} \quad \left(R_H = \frac{1}{ne} \text{ and } \sigma = \frac{1}{9}\right)$$

$$\mu = \sigma R_H = \frac{R_H}{\rho} = \frac{3.66 \times 10^{-4}}{8.93 \times 10^{-3}}$$

$$\mu = \mathbf{0.0409\ m^2/volt\ sec}$$

Problem 1.10: *A semiconductor crystal 12 mm long, 1 mm wide and 1 mm thick has a magnetic flux density of 0.5 wb/m^2 applied from front to back, perpendicular to largest faces. When a current of 20 mA flows length wise through the specimen, the voltage measured across, its width is found to be 37μ volts. What is the Hall coefficient of semiconductor?*

Solution: Given: Semiconducting crystal

Length (L) = 12 mm = 12×10^{-3} m

Thickness (t) = 1 mm = 1×10^{-3} m

Breadth (b) = $1\ mm = 1 \times 10^{-3}\ m$

Current (I) = $20\ mA = 20 \times 10^{-3}\ A$

Hall voltage (V_H) = $37\ \mu V = 37 \times 10^{-6}\ V$

Magnetic flux density (B) = $0.5\ Wb/m^2$

Formula: Hall voltage (V_H)

$$V_H = \frac{BWJ}{ne} = \frac{BWI}{neA}$$

Let t be thickness, w be the width of the sample, then A = Wt

$$V_H = \frac{BWI}{neWt} = \frac{R_H BI}{t}$$

$$R_H = \frac{V_H \times t}{I \times B}$$

$$R_H = \frac{37 \times 10^{-6} \times 1 \times 10^{-3}}{20 \times 10^{-3} \times 0.5}$$

$$R_H = \mathbf{3.7 \times 10^{-6}\ m^3/c}$$

Problem 1.11: *A bar of n-type Ge of size 0.010 m × 0.001 m × 0.001 m is mounted in a magnetic field of 2×10^{-1} T. The electron density in the bar is $7 \times 10^{21}/m^3$. If one mili-volts is applied across the long ends of the bar, determine the current through the bar and the voltage between Hall electrodes placed across the short dimensions of the bar.*

Solution: Assume $\mu_n = 0.39\ m^2/vsec$ $B = 2 \times 10^{-1}$ T, $n = 7 \times 10^{21}/m^3$

Formula:
$$\rho = \frac{1}{\mu_n e} = \frac{1}{0.39 \times 7 \times 10^{21} \times 1.6 \times 10^{-19}}$$

$$= 2.28 \times 10^{-3}\ \Omega/m$$

Now
$$R = \frac{\rho l}{A} = \frac{2.28 \times 10^{-3} \times 0.01}{(0.001 \times 0.001)}$$

$$R = \mathbf{22.8\ \Omega}$$

Using ohm's law
$$I = \frac{V}{R} = \frac{1 \times 10^{-3}}{22.8} = 4.385 \times 10^{-5}$$

$$= \mathbf{43.85\ \mu A}$$

Using formula for Hall voltage, $V_H = R_H BJW$, As $R_H = \rho \times \mu$

and
$$J = \frac{I}{A} = \frac{I}{W \times t}$$

$$V_H = \rho \times \mu \times B = \frac{I}{WL} \times t = [\rho \mu I\ B\ /W]$$

$$= \frac{2.28 \times 10^{-3} \times 0.39 \times 0.2 \times 43.85 \times 10^{-6}}{0.001}$$

$$V_H = 7.798 \times 10^{-6}\ \mu V$$

$$V_H = \mathbf{7.798\ \mu V}$$

Problem 1.12: *In a semiconductor with Hall coefficient 145 cc/c having width 2 cm and thickness 0.2 cm with a magnetic field induction of 2T along the smaller dimension, a current of 150 mA is calculated the current density and Hall voltage.*

Solution: Given: Hall coefficient, $R_H = 145$ cc/c, $I = 150$ mA

Width $w = 2$ cm, Thickness $t = 0.2$ cm, Magnetic field $B = 2T$

Current density $$J = \frac{I}{A} = \frac{I}{w \times d} = \frac{150 \times 10^{-3}}{2 \times 10^{-2} \times 0.2 \times 10^{-2}}$$

$$\mathbf{J = 3750\ A/m^2}$$

Now, Hall co-efficient,

$$R_H = \frac{V_H/d}{JB}, \quad V_H = R_H JB$$

Now, $$w = 145 \times 10^{-6} \times 3750 \times 2 \times 0.2 \times 10^{-2} = 2.175 \times 10^{-3}\ V$$

$$\mathbf{w = 2.175\ mV}$$

Problem 1.13: *Suppose a pure Si crystal has 5×10^{28} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}\ m^{-3}$.*

Solution: Note that thermally generated electrons ($n_i \sim 10^{16}\ m^{-3}$) are negligibly small as compared to those produced by doping.

Therefore, $n_e \approx ND$.

Since $n_e n_h = n_i^2$

The number of holes,

$$n_h = \frac{(2.25 \times 10^{32})}{(5 \times 10^{22})}$$

$$= \mathbf{4.5 \times 10^9\ m^{-3}}$$

UNIVERSITY QUESTIONS

1. What is Fermi level and Fermi energy? Write Fermi Dirac distribution function and explain the terms used in it. **(M.U. May 2011, Dec. 2009, 2012, 2013, 2016, 2024)**
2. Show that for an intrinsic semiconductor, Fermi level lies in the middle of forbidden band. **(M.U. May 2013, Dec. 2009, 2010, 2012, 2013, 2015, 2016, 2024)**
3. Show how the Fermi level shifts with increasing temperature in n-type semiconductors. **(M.U. May 2013, Dec. 2010, 2016)**
4. How does the position of the Fermi energy level change with increasing doping concentration in P-type semiconductors? Sketch the diagram. **(M.U. Dec. 2016)**
5. How does the position of the Fermi energy level change with increasing doping concentration in N-type semiconductors? Sketch the diagram. **(M.U. Dec. 2016)**
6. Explain concept of Fermi level. Prove that Fermi level is exactly at center of forbidden energy gap in an intrinsic semiconductor. **(M.U. May 2017, 2024)**

7. The electrical conductivity of a pure silicon at room temperature is 4×10^{-4} mho/m. If the mobility of the electron is 0.14 m^2/V-S and that of the hole is 0.04 m^2/V-S, calculate the intrinsic carrier density. **(M.U. May 2017)**
8. What is the probability of an electron being thermally excited to the conduction band in Si at 30°C? The band gap energy is 1.12 eV. **(M.U. May 2018)**
9. With an energy band diagram, explain variation of the Fermi energy level with temperature in an extrinsic semiconductor. **(M.U. Dec. 2017)**
10. With an energy band diagram, explain variation of the Fermi energy level with impurity concentration in an extrinsic semiconductor. **(M.U. May 2018)**
11. With the help of the diagram, explain the effect of impurity concentration on the Fermi level of a P-type semiconductor. **(M.U. Dec. 2019)**
12. With the help of a diagram, explain the effect of impurity concentration on Fermi level of N-type semiconductor. **(M.U. Dec. 2019)**
13. What is the probability of an electron being thermally excited to conduction band in Silicon at 20°C if the bandgap is 1.12 eV? ($k = 8.6 \times 10^{-5}$ eV/K) **(Dec. 2023)**

PRACTICE PROBLEMS

1. An electric field of 100 V/m is applied to a sample of n-type semiconductor whose Hall coefficient is –0.0125 m^3/c. Determine the current density in the sample. Assume $\mu e = 0.6$ m^2/v.s.

Ans. $J = -2880C\ km^2 = -2880\ A/m^2$

2. A copper strip 2.0 cm wide and 1.0 mm thick is placed in a magnetic field with $B = 1.5$ wb/m^2. If a current of 200 A is setup in the strip, calculate Hall voltage that appears across the strip. Assume $R_H = 6 \times 10^{-7}$ m^3/c.

Ans. $V_H = 0.18$ V

3. The resistivity of intrinsic InSb at room temperature is 2×10^{-4} Ω cm. If the mobility of the electron is 6 m^2/V-sec and the mobility of hole is 0.2 m^2/V sec, calculate its intrinsic carrier density.

Ans. $n_i = 5.04 \times 10^{23}/m^3$.

4. In an n-type semiconductor, the Fermi level lies 0.4 eV below the conduction band. If the concentration of the donor atom is doubled, find the new position of the Fermi level w.r.t. the conduction band.

Ans. $E_c - E_F = 0.382$ Ev

QUESTIONS

1. Pure silicon semiconductor at 500 K has equal electrons and holes (1.5×10^{16} m^{-3}). Doping by indium increases n_h to 4.5×10^{22} m^{-3}. Calculate the type and electron concentration of the doped semiconductor.
2. In an intrinsic semiconductor, the number of conduction electrons is 7×10^{19} m^3. Find the total number of current carriers in the same semiconductor of size 1 cm × 1 cm × 1 mm.
3. The intrinsic carrier density is $1.5 \times 10^{16}/m^3$. If the electron and hole mobilities are 0.13 and 0.05 $m^2v^{-1}s^{-1}$. Calculate its electrical conductivity.

4. The energy gap of silicon is 1.14 eV. What is the maximum wavelength at which silicon will begin absorbing energy?
5. Find intrinsic carrier concentration and Position of Fermi energy level in Silicon with respect to the VB edge. Given m_h = 0.92 me; m_e = 0.49 mo. N_c = 2.21 × 1025 /m^3 and N_v = 8.60 × 1024/m^3 and T = 300 K
6. In an intrinsic semiconductor with Eg = 0.7 eV, Determine the position of the Fermi level at T = 300 K if mp* = 6me*. Also calculate the density of holes and electrons at 300 K. How do these quantities alter if Eg = 7 eV?
7. In a pure semiconductor, the number of electrons is $6 \times 10^{19}/m^3$. How many holes are there on a sample of size 1 cm × 1 cm × 1 mm?
8. The band gap for Si is 1.1 eV. (a) Find ratio of band gap to kT for silicon at room temperature 300 K. (b) At what temperature does this ration becomes one tenth of value at 300 K.
9. A bar of n-type Ge of size 0.001 m × 0.001 m × 0.001 m is mounted in a magnetic field of 5×10^{-1} T. The electron density in the bar is $7 \times 10^{21}/m^3$. If one mili-volts is applied across the long ends of the bar, determine the current through the bar and the voltage between Hall electrodes placed across the short dimensions of the bar.
10. A bar of n-type Ge of size 0.002 m × 0.002 m × 0.002 m is mounted in a magnetic field of 2.5×10^{-1} T. The electron density in the bar is $7 \times 10^{21}/m^3$. If one mili-volts is applied across the long ends of the bar, determine the current through the bar and the voltage between Hall electrodes placed across the short dimensions of the bar.
11. A bar of n-type Si of size 0.002 m × 0.002 m × 0.002 m is mounted in a magnetic field of 5×10^{-1} T. The electron density in the bar is $7 \times 10^{21}/m^3$. If one mili-volts is applied across the long ends of the bar, determine the current through the bar and the voltage between Hall electrodes placed across the short dimensions of the bar.
12. The concentration of conduction electrons in germanium is $6 \times 10^{19}/m^3$. When some phosphorus impurity is domed into germanium sample, the concentration of electron increases to $2 \times 10^{23}/m^3$. Find the concentration of holes in doped germanium.
13. The effective mass of holes and electrons in GaAs are respectively 0.48 and 0.067 times the free electron mass. The band gap energy is 1.43 eV. How much above is its fermi-level from the top of the valence band at 300 K?
14. The effective mass of conduction electron in Si is 0.31 times the free electron mass. Find conduction electron density at 300 K, Assume: Fermi level lies exactly at center of energy band gap (= 1.11 eV).
15. In intrinsic GaAs, effective masses of electron and hole respectively are 0.068 and 0.50 times the electron mass. The energy band gap is 1.43 eV. Determine carrier density at 300 K.
16. Why valence band in semiconductors partially empty and the conduction band is partially filled at room temperature?
17. Explain (or sketch) temperature dependence of resistance for semiconductors. Why does resistance of a semiconductor decrease with increasing temperature?

18. What are the basic steps used to derive the Fermi-Dirac distribution?
19. What is the physical significance of the Fermi energy?
20. How does the position of Fermi level with respect to band structure?
21. Describe the two types of semiconductors and contrast their conduction mechanism.
22. Why Does the Resistivity of Semiconductors Go Down with Temperature?
23. With neat sketches, explain how Fermi level varies with impurity concentration and temperature in both p-type and n-type semiconductors.
24. What is Hall Effect? Describe an experimental arrangement to measure the Hall coefficient.
25. Assuming the Fermi-Dirac distribution, derive or State an expression for the concentration of electrons per unit volume in conduction band of an intrinsic semiconductor.
26. State Limitations of intrinsic semiconductor.
27. Give its importance of Fermi energy. Write down expression for Fermi Distribution function.
28. Give the expression for the carrier concentration in semiconductor.
29. Why? Silicon is widely used to manufacture the elemental device Compared with Germanium.
30. Draw the graph for variation of Fermi level with temperature in p -type semiconductor.
31. Define Fermi level in case of semiconductors. Mention its position in intrinsic and extrinsic semiconductors at 0 k.
32. What is Fermi level? Prove that the Fermi level is lies exactly in between conduction band and valance band of intrinsic semiconductor.
33. What are the properties of semiconductor?
34. What is intrinsic semiconductor and explain formation of extrinsic semiconductors through doping?
35. Derive expression for current generated due to drifting of charge carriers in semiconductors in the presence of electric field.
36. Obtain the conductivity of intrinsic semiconductor with relevant expressions?
37. Distinguish between intrinsic and extrinsic semiconductors?
38. Explain effect of temperature on Fermi energy level of an extrinsic semiconductor?
39. Explain the role of density states.
40. What do you understand by extrinsic semiconductor.
41. Draw the energy level diagram to show effect of temperature and effect of impurity concentration in P and N-type semiconductors.
42. Explain How to calculate Hall voltage?
43. State at least any four applications of the Hall Effect?
44. Why is Silicon preferred over germanium in the manufacture of semiconductor devices?
45. Explain application of Hall voltage?

Module - II

JUNCTION DIODE

Syllabus:

- *Formation of p-n junction, Calculation of barrier potential, Diode equation, p-n junction in forward bias, p-n junction in reverse bias, Current- voltage curve for p-n junction diode, LED and it's working.*

Objectives:

- *To explain the basic importance of p-n junction diodes.*

Outcome:

- *Learners will be able to Calculate barrier potential and Plot I-V characteristics of p-n junction diodes.*

List of Contents:

2.1 *Introduction to Junction Diode*

2.2 *Formation of p-n Junction*

2.3 *Calculation of Barrier Potential*

2.4 *Diode Equation*

- 2.4.1 *Diode Equation in Forward Biased*
- 2.4.2 *Diode Equation in Reverse Biased*
- 2.4.3 *Diode Equation at Room Temperature*

2.5 *Biasing of Diode*

- 2.5.1 *p-n Junction in Forward Bias*
- 2.5.2 *p-n Junction in Reverse Bias*

2.6 *Current- Voltage Curve for p-n Junction Diode*

2.7 *LED and its Working*

2.8 *Application of Junction Diode*

2.9 *Numericals*

- *Questions*

2.1 INTRODUCTION TO JUNCTION DIODE

A structure made with P and N-type materials is generally known as a **junction diode**. It is regarded as a two-terminal device. The common point where these materials are connected is called a **junction**. A junction diode allows current carriers to flow in one direction and obstructs the flow of current in the reverse direction.

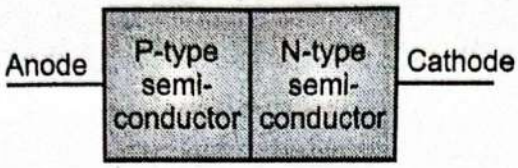


Fig. 2.1: P-N Junction

The above Fig. 2.1 shows the crystal structure of a junction diode. Let us look the location of P-type and N-type materials with respect to the junction. The structure of crystal is continuous from one end to the other. The junction acts only as a separating point that represents the end of one material and the beginning of the other. Such structure allows the electrons to move thoroughly in the entire structure.

2.2 FORMATION OF P-N JUNCTION

In a piece of silicon, if one half is doped by p-type impurity and the other half is doped by n-type impurity, a PN junction is formed. The plane dividing the two halves is called a ***PN junction****.*

As specified, each part of material as **majority** and **minority current carriers**. i.e. n-type material has a high concentration of free electrons while p-type material has a high concentration of holes.

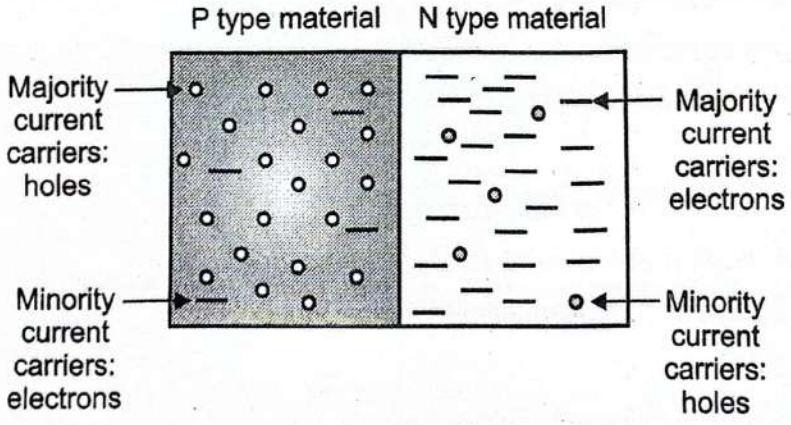


Fig. 2.2: Majority and minority current carriers in p-n junction diode

As we know and seen in above Fig. 2.2, in N-type material, electrons are the majority carriers and holes are the minority carriers. In P-type material, holes are the majority carriers and electrons are the minority.

Initially, when a junction diode is formed, there is a unique interaction between current carriers. Therefore, at the junction there is a tendency of free electrons to diffuse over to the P side and the holes to the N side. This process is called **diffusion**. Diffusion is the result of high accumulation of carriers in one material and a lower gathering in the other.

Generally, the current carriers which are near to the junction only takes part in the process of diffusion. Electrons departing the N material cause positive ions to be generated in their place. While entering the P material to fill holes, negative ions are created by these electrons. As a result, each side of the junction contains a large number of positive and negative ions.

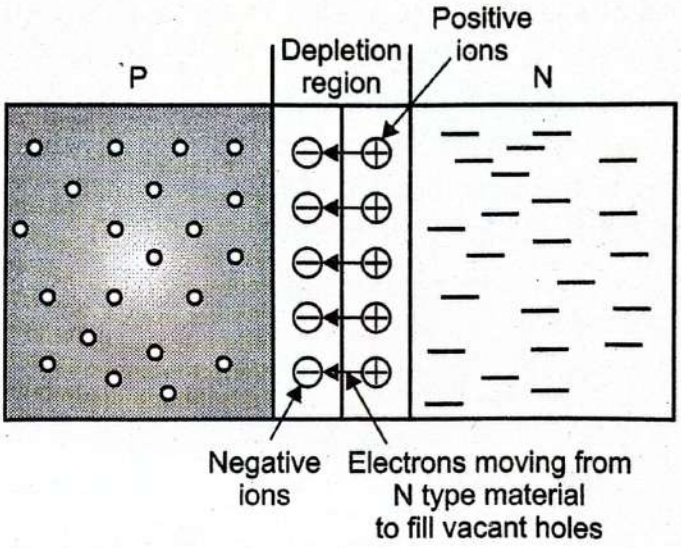


Fig. 2.3: Depletion region of a junction diode

The area where these holes and electrons become depleted is generally known by the term **depletion region**. It is an area where there is lack of majority current carriers. Normally, a depletion region is developed when P-N junction is formed. The Fig. 2.3 shows the depletion region of a junction diode.

Fermi Level in an Unbiased p-n Junction

- When a p-n junction is formed in the p-type, there is an excess of holes and the Fermi level E_{FP} is near to the valence band, also in the n-type. There is excess of electrons and the Fermi level is below the conduction band in an unbiased situation.
- As the junction is formed, diffusion starts, electrons from the conduction band of n-type diffuse through the junction to the p-side. Similarly, holes from the valence band of p-type diffuse to n-type.

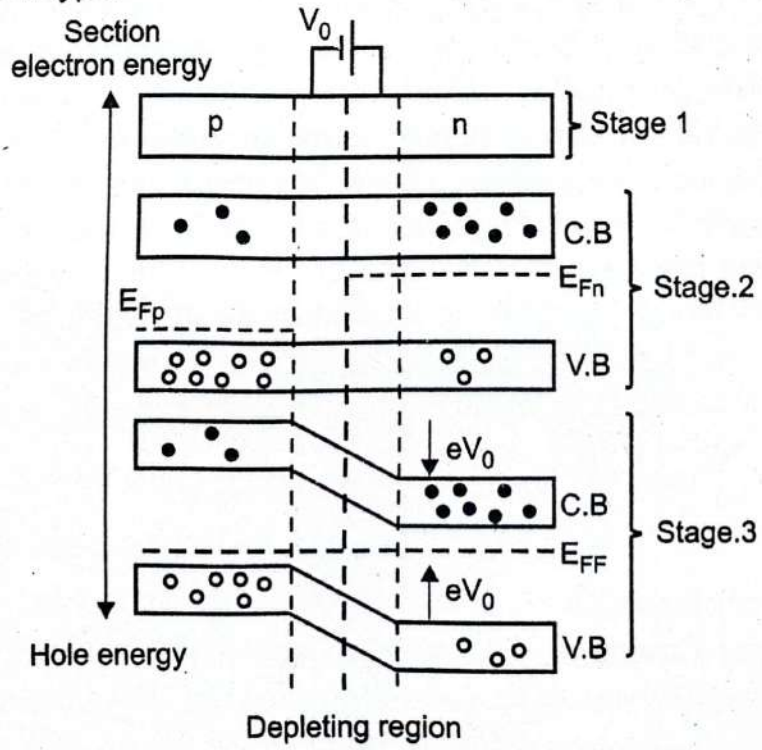


Fig. 2.4: Fermi level in an unbiased p-n junction

- As the concentration of electrons increases in the conduction band of p-type, Fermi level E_{FP} starts moving upwards along with the entire p-type energy band structure. Similarly, more holes entering the valence band of n-type Fermi level E_{Fn} move downwards. The energy band structure also moves downwards. Finally, a stage comes when the charge density on both sides of the same baud is uniform. And thus, the Fermi levels TE_{Fn} and E_{FP} under equilibrium conditions align with each other.
- Under equilibrium conditions, the conduction band and valence bands of both sides are positioned such that a conduction hill of height $-eV_0$ and a valence hill of height eV_0 are formed. There are the potential energies of the electrons and holes due to the potential barrier V_0. The process is explained in three stages as shown in Fig. 2.4, thus forming the Depletion region.

2.3 CALCULATION OF BARRIER POTENTIAL

As the free electrons move across the junction from N-type to P-type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling the holes. Therefore, a negative charge is developed on the p –side of junction. This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly, the net positive charge on the N side repels the holes crossing from the p side to the N side. Thus a barrier is set up near the junction that prevents the further movement of charge carriers i.e., electrons and holes.

The immobile ions (negative acceptor ions and positive donor ions) are concentrated between the N and P-region and create the electric field, which acts as a barrier between the flows of charges. The region is created because of the depleted ions and hence it is called the **depletion region**. The depletion region acts as a barrier and opposes the flow of charge carrier.

Calculation of Barrier Potential of a PN Junction Diode

As a consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between the P and N regions, termed as **barrier potential** (or junction barrier or diffusion potential or contact potential) $\mathbf{V_0}$. The barrier in which the charge carrier stopped by the obstructive force is termed as **barrier potential.** The magnitude of these potential V_0 varies with doping levels and temperature in semiconductor. The barrier potential for germanium is approximately 0.3 V and for silicon, it is 0.7 V. These values cannot be measured directly and appears across the space charge region of the junction. In order to produce current conduction, the barrier potential of a P-N junction must be overcome by an external voltage source.

The barrier potential is a critical parameter in semiconductors. It is given mathematically,

$$V_{bi} = \frac{kT}{q} ln\left[\frac{N_A N_D}{\eta_i^2}\right]$$

where,

V_{bi} is the barrier potential (V).
k is the Boltzmann constant.
T is the absolute temperature (in Kelvin).
q is the elementary charge (1.602×10^{-19} C).

N_A is the acceptor doping concentration (cm^{-3}).

N_D is the donor doping concentration (cm^{-3}).

n_i is the intrinsic carrier concentration (cm^{-3}).

In the above equation, the **logarithmic term** reflects the ratio of doping concentrations to the intrinsic carrier concentration, thus determining the magnitude of barrier potential. And the term **kT/q** is known as thermal voltage which is approximately 26 mV at room temperature (300 k).

Significance of Barrier Potential

- **Diode Functionality:** The barrier potential determines the voltage required to overcome the potential barrier in a p-n junction, allowing significant current flow in the forward direction.
- **Depletion Region:** It influences the width of the depletion region and the electric field within the p-n junction.
- **Device Performance:** Understanding and calculating the barrier potential is essential for designing and analyzing devices such as diodes and transistors.

2.4 DIODE EQUATION

The Diode equation can be derived by assuming the depletion width is zero. When a diode is forward biased, holes are injected from the p-side into the n-side, increasing the concentration of holes, denoted as p in the n-side.

This equation shows the relationship between current flowing through diode as a function of the applied voltage. This equation also known as a Shockley equation or diode law, named after transistor co-inventor William Shockley of Bell Labs. Mathematically Diode equation is as,

$$I = I_o\left[e\left(\frac{qV}{\eta kT}\right) - 1\right]$$

where, I = current flowing through the diode

I_o = reverse saturation current

q = charge of the electron

V = voltage applied across the diode

η = exponential ideality factor of the diode

K = Boltzmann constant and $K = 1.38 \times 10^{-23}$ J/K

T is the absolute temperature in Kelvin

The current flowing through diode does not vary linearly with an increase in applied voltage. The V-I characteristics of diode have an exponential relationship. The diode resistance varies with an increase in the temperature. As a result, the current does not vary linearly with voltage. The diode is a non-ohmic and nonlinear semiconductor device.

2.4.1 Diode Equation in Forward Biased

When the diode is in a forward-biased condition, a large forward current flows through it, and the value of the exponent term is more significant.

$$I = I_o\left[e\left(\frac{V}{kT}\right) - 1\right]$$

$$\therefore \quad \frac{e^V}{\eta V_T} >> 1$$

The diode current equation in forward bias becomes

$$I = I_o\, e^{\frac{qV}{\eta KT}}$$

2.4.2 Diode Equation in Reverse Biased

When the diode is reverse-biased, the exponential term becomes negligible, and the diode current is equal to the reverse saturation current.

$$I = I_o\left[e\left(\frac{V}{kT}\right) - 1\right]$$

$$\therefore \quad \frac{e^V}{\eta V_T} << 1$$

$$I = -I_o$$

2.4.3 Diode Equation at Room Temperature

At room temperature, the behavior of diode is affected by the thermal voltage that can be calculated below:

Let, $T = 27°C.$

Temperature in Kelvin (T) = 27 + 273 = 300 K,

$$k = 1.38 \times 10^{-23}\ JK^{-1}$$

$$q = 1.6 \times 10^{-19}\ C$$

$$V = (kT/q) = 0.02587 = 25.87\ mV$$

Thus thermal voltage is as approximately 25.87mV.

$$I = I_o\, e^{\frac{V}{0.025 \times \eta}}$$

2.5 BIASING OF DIODE

The term bias refers to the application of DC voltage to set up certain operating conditions or when an external source of energy is applied to a P-N junction, it is called a bias voltage or simply biasing. This method either increases or decreases the barrier potential of the junction. As a result, the reduction of the barrier potential causes current carriers to return to the depletion region. In a junction diode there are two operational regions: (i) p-type and (ii) n-type. It is biased in two forward and reverse ways.

1. **Forward Biasing:** An external voltage is added of the same polarity to the barrier potential, which causes an increase in the width of the depletion region. In other words, p-type is connected to the positive terminal of the voltage potential, while the n-type is connected to the negative terminal.

2. **Reverse Biasing:** A PN junction is biased in such a way that the application of external voltage action prevents current carriers from entering the depletion region. In other words, p-type is connected to the negative terminal of the voltage potential, while the n-type is connected to the positive terminal.

2.5.1 p-n Junction in Forward Bias

The p-n junction is said to be forward-biased when the p-type is connected to the positive terminal of the battery and the n-type connected to the negative terminal of the battery. In forward bias, built-in electric field at the junction and the applied electric field are in opposing directions. The resulting electric field is smaller than the built-in electric field when both electric fields are added together. As a result, the depletion area becomes less resistant and thinner. i.e., potential barrier is reduced when the diode is placed in this fashion. When the applied voltage is high, the resistance of the depletion area becomes insignificant.

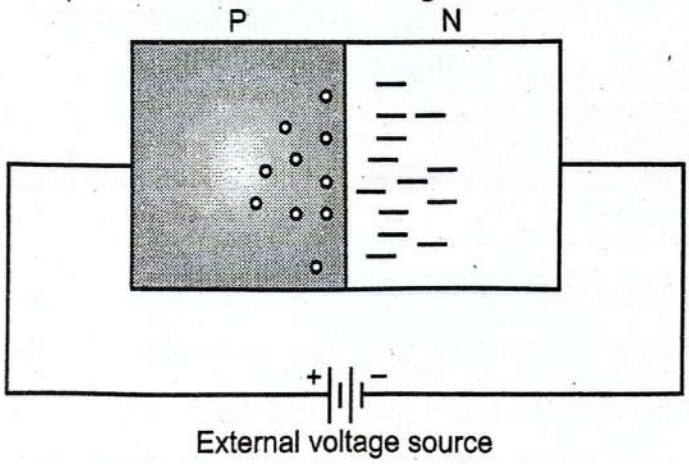


Fig. 2.5: Forward biased P-N junction diode with majority carriers

At 0.67 V, the resistance of the depletion area in silicon (or at 0.295 V in germanium) becomes absolutely insignificant, allowing current to flow freely over it. When the applied voltage is 0.7 V for silicon diodes (or 0.30 V for germanium diodes) the potential barriers fall, and current flows. The current grows slowly while the diode is under forward bias, and the curve formed is non-linear as the voltage supplied to the diode overcomes the potential barrier. Once the diode has crossed the potential barrier, it functions normally, and the curve rises quickly as the external voltage rises, yielding a linear curve.

From, Fig. 2.5,

- This bias voltage repels the majority current carriers of each P and N-type material. As a result, large number of holes and electrons start appearing at the junction.
- At the N-side of the junction, electrons move in to neutralize the positive ions in the depletion region.
- On the P-side material, electrons are dragged from negative ions, which cause them to become neutral again. This means that forward biasing collapses the depletion region and hence the barrier potential too. It means that when P-N junction is forward biased, it will allow a continuous current flow.

The following Fig. 2.6 shows the flow of current carriers of a forward-biased diode. A constant supply of electrons is available due to an external voltage source connected to the diode. The flow and direction of the current are shown by large arrows outside the diode in the diagram. Note that the electron flow and the current flow refer to the same thing.

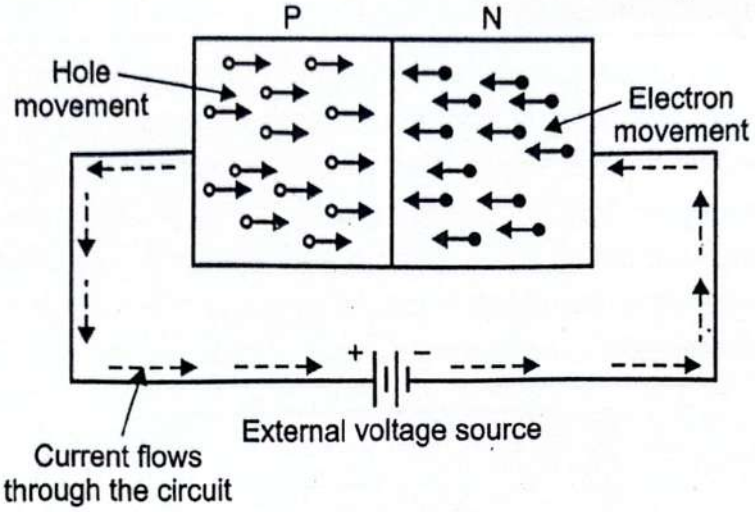


Fig. 2.6: Forward biased P-N junction diode with flow of charges

From, Fig. 2.6,

- Suppose electrons flow through a wire from the negative battery terminal to the N material. Upon entering this material, they flow immediately to the junction.
- Similarly, on the other side, an equal number of electrons are pulled from P side and are returned to the positive battery terminal. This action creates new holes and causes them to move toward the junction.
- When these holes and electrons reach the junction, they join together and effectively disappear. As a result, new holes and electrons emerge at the outer ends of the diode. These majority carriers are created on a continuous basis. This action continues as long as the external voltage source is applied.
- When a diode is forward biased, it can be noticed that electrons flow through the entire structure of the diode. This is common in N-type material, whereas in the P material holes are the moving current carriers. There, to have holes movement in one direction must begin by electron movement in the opposite direction. Therefore, the total current flow is addition of holes and electrons flow through a diode.

Forward Bias p-n Junction

- With forward biasing of the p-n junction, electron density in the conduction band of n-type increases, resulting in upward movement of the Fermi level E_{Fn}. Similarly, there is an increase in hole density in the valence band of the p-type resulting in downward movement of the Fermi level E_{Fp} in the p-type.
- Thus, due to the applied voltage V, there is a displacement by an amount eV in the Fermi levels E_{Fn} and E_{Fp}.

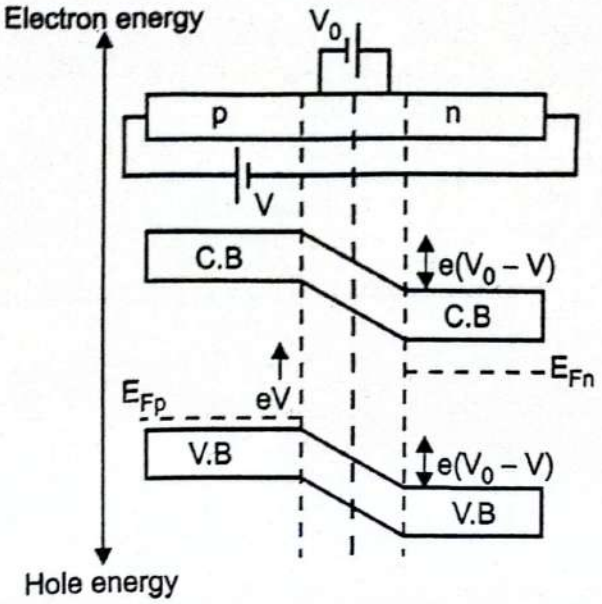


Fig. 2.7: Fermi level in forward bias p-n junction

- There is a reduction in the height of conduction hill by eV, resulting in e (V_0 – V). Similarly, the height of the valence hill becomes –e (V_0 – V). Thus, making the depletion region smaller and charge flow easier across the junction shown in Fig. 2.7.

2.5.2 p-n Junction in Reverse Bias

The following Fig. 2.8 shows reverse biased PN junction diode with external voltage applied. The p-n junction is said to be reverse-biased when the p-type is connected to the negative terminal of the battery while the n-type is connected to the positive terminal of battery. Note that in such an arrangement, battery polarity is to oppose the material polarity of the diode so that dissimilar charges attract. Hence, majority charge carriers of each material are dragged away from the junction. Reverse biasing causes the diode to be nonconductive.

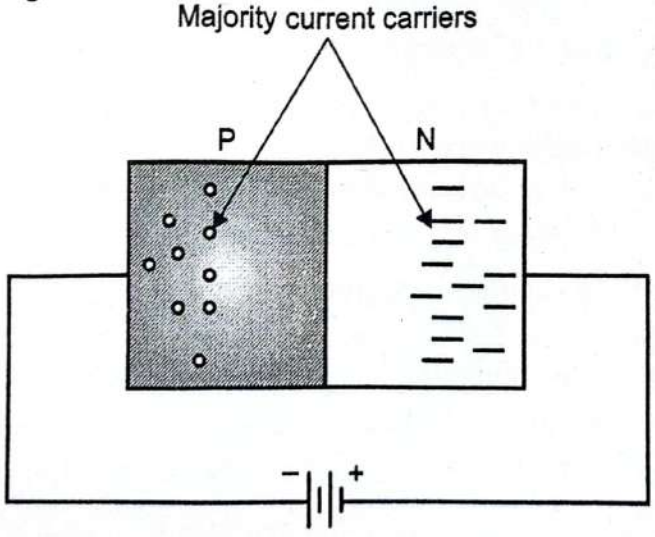


Fig. 2.8: Reverse biased P-N junction diode with majority carriers

From, Fig. 2.8,

- When the PN junction diode is under negative bias, the p-type is linked to the negative terminal of the external voltage, while the n-type is connected to the positive terminal. As a result, the potential barrier becomes higher. Because minority carriers are present at the junction, a reverse saturation current occurs at first.

- When applied voltage is raised, the kinetic energy of the minority charges increases, affecting the majority charges. This is the point at which the diode fails. The diode may be destroyed as a result of this.

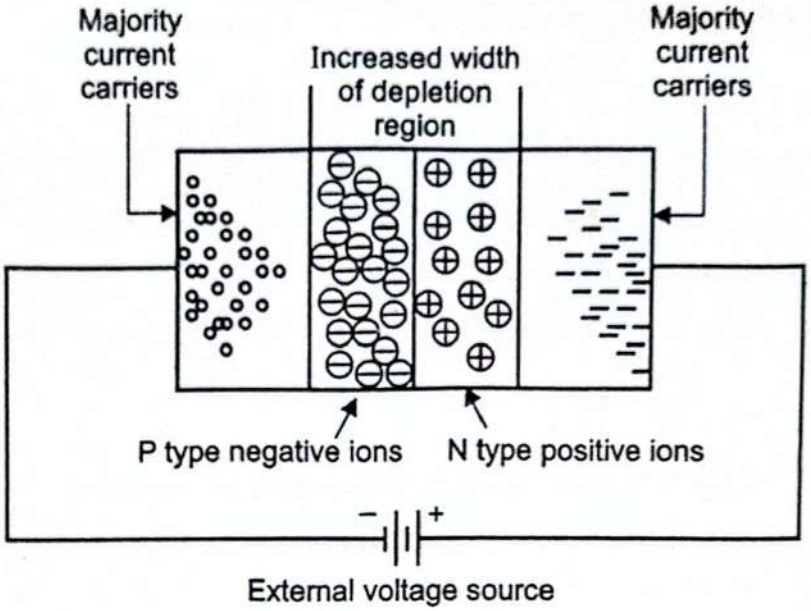


Fig. 2.9: Reverse biased P-N junction diode with flow of charges

From, Fig. 2.9,

- Due to circuit action, electrons of the N material are pulled toward the positive battery terminal.
- Each electron that moves or departs the diode causes a positive ion to emerge in its place. As a result, this causes an equivalent increase in the width of the depletion region on the N side of the junction.
- The P side of the diode has a similar effect to the N side. In this action, a number of electrons leave the negative battery terminal and enter the P-type material.
- These electrons then straight away move in and fill a number of holes. Each occupied hole then becomes a negative ion. These ions in turn are then repelled by the negative battery terminal and driven toward the junction. Due to this, there is an increase in the width of the depletion region on the P side of the junction.
- The overall width of the depletion region directly depends on an external voltage source of a reverse-biased diode. In this case, the diode cannot efficiently support the current flow through the wide depletion region. As a result, the potential charge starts developing across the junction and increases until the barrier potential equals the external bias voltage. After this, the diode behaves as a nonconductor.

Reverse Bias p-n Junction

- On reverse biasing, electrons from the conduction band of p-sides are repelled by the negative polarity of the applied potential difference, V and diffuse through the junction. Thus increasing the concentration of electrons in the conduction band of n-type.
- As the conduction band of p-type gets an excess population of electrons, the Fermi level E_{Fp} moves upwards. Similarly, the valence band of n-type receives excess holes. Hence, the Fermi level E_{Fn} shift downwards.

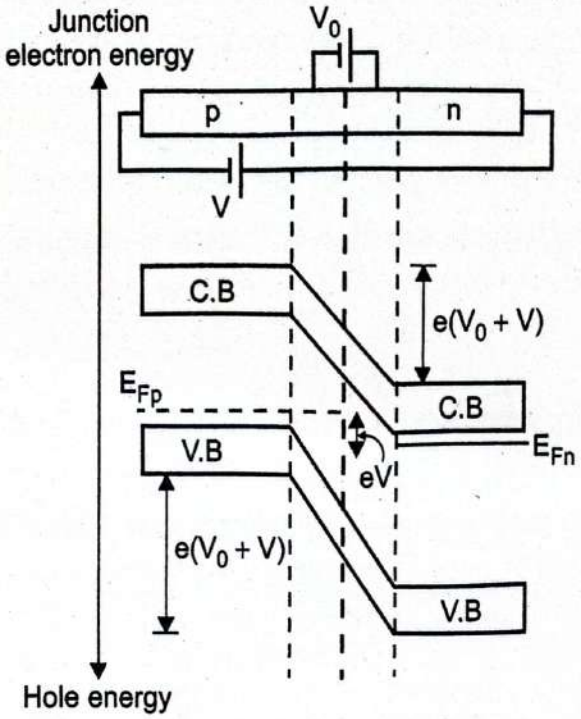


Fig. 2.10: Fermi level in reverse bias p-n junction

- The relative displacement of the Fermi level E_{Fp} and E_{Fn} is equal to eV, which is the potential energy due to potential difference V.
- The equilibrium condition is achieved when the conduction hill of height $-e\ (V_0 + V)$ and the valence hill of height $e\ (V_0 + V)$ are formed.
- With an increase in the height of the barrier region, current flow reduces through the junction. Thus producing the reverse current by minority charge carrier as shown in Fig. 2.10.

2.6 CURRENT- VOLTAGE CURVE FOR P-N JUNCTION DIODE

There are diverse current scales for forward bias and reverse bias operations. This curve indicates that the diode conducts simply when the P-region is made positive and the N-region negative. The diode conducts almost no current in the high resistance direction, i.e., when the P region is made negative and the N region is made positive. Now the holes and electrons are drained away from the junction, causing the barrier potential to increase. This condition is indicated by the reverse current portion of the curve.

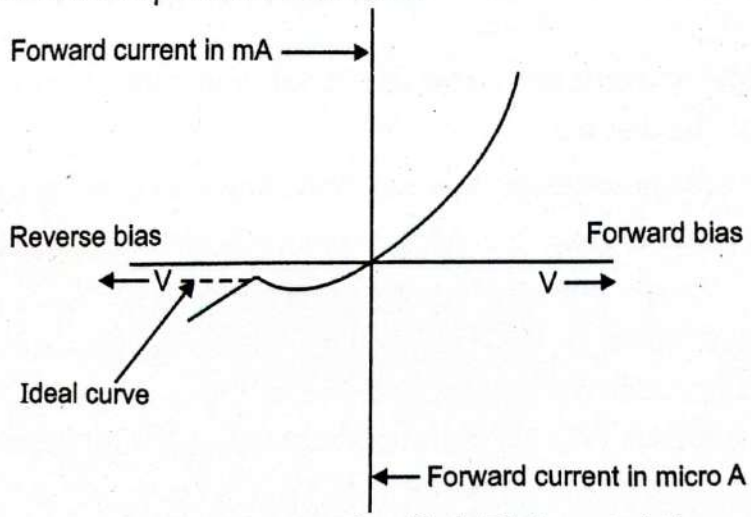


Fig. 2.11: Ideal PN junction diode IV characteristics

The dotted section of the curve (Fig. 2.11) indicates the **ideal curve**, which would result if it were not for avalanche breakdown. The following Fig. 2.12 shows the static characteristic of a PN junction diode.

Diode IV Characteristics

The Fig. 2.12 depicted under the section Forward Characteristic shows that Forward Voltage and Reverse Voltage are usually plotted on the horizontal line of the graph. Forward and reverse current values are shown on the vertical axis of the graph. Forward voltage is represented to the right and reverse voltage to the left. The point of beginning or zero value is at the center of graph. Forward Current lengthens above the vertical (y-axis) and Reverse Current extending downward (y-axis).

A curve between the voltage and the current across the circuit defines the V-I properties of p-n junction diodes. The x-axis represents voltage, while the y-axis represents current. The V-I characteristics curve of the p-n junction diode is shown in Fig. 2.12.

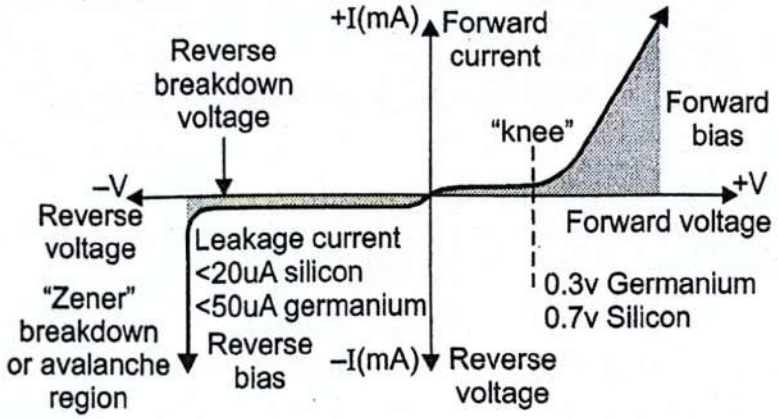


Fig. 2.12: Typical PN junction diode I-V characteristics

Forward IV-Characteristics

When a diode is forward biased, it conducts current (I_F) in forward direction. The value of I_F is directly dependent on the amount of forward voltage. The relationship of forward voltage and forward current is called the ampere-volt characteristic of a diode. A typical diode forward IV characteristic is shown in Fig. 2.12.

From Fig. 2.12,

- Forward voltage is measured across the diode and forward current is a measure of current through the diode.
- When forward voltage across a diode equals 0V, forward current equals to 0 mA.
- When the value starts from the starting point (0) of the graph, if V_F is progressively increased in 0.1 V steps, I_F begins to rise.
- When the value of V_F is large enough to overcome the barrier potential of the P-N junction, a considerable increase in IF occurs. The point at which this occurs is often called the knee voltage ($\mathbf{V_K}$). For $\mathbf{V_K}$ is approximately 0.3 V for germanium, and 0.7 V for silicon diodes.
- If the value of IF increases much beyond $\mathbf{V_K}$, the forward current becomes quite large.

Reverse I-V Characteristics

When a diode is reverse biased, it conducts reverse current that is usually quite small. A typical diode reverse I-V characteristic is shown in Fig. 2.12. The vertical reverse current line in this graph has current values expressed in microamperes. The amount of minority current carriers that take part in the conduction of reverse current is quite small. In general, this means that reverse current remains constant over a large part of reverse voltage.

When the reverse voltage of a diode is increased from the start, there is a very slight change in the reverse current. At the breakdown voltage (V_{BR}) point, current increases very rapidly. The voltage across the diode remains reasonably constant at this time.

This IV characteristic leads to a number of applications of diodes under reverse bias condition. The processes that are responsible for current conduction in a reverse-biased diode are called **Avalanche breakdown** and **Zener breakdown**.

2.7 LED AND ITS WORKING

LED (Light Emitting Diode) *is an optoelectronic device that works on the principle of electro-luminance.* ***Electro-luminance*** *is the property of a material to convert electrical energy into light energy and later it radiates this light energy. LEDs* are directly or indirectly influencing our day-to-day activities such as message display on LED TVs, everywhere these LEDs exist.

If LEDs are made from Silicon and Germanium, then during recombination of electrons, all the energy is dissipated in the form of heat only. On the other hand, materials such as Gallium Arsenide (GaAs) and Gallium Phosphide (GaP) possess enough photons that are sufficient to produce visible light.

If LEDs are made from gallium arsenide, they produce red light.

If LEDs are made from Gallium Phosphide, then such LEDs emit green light.

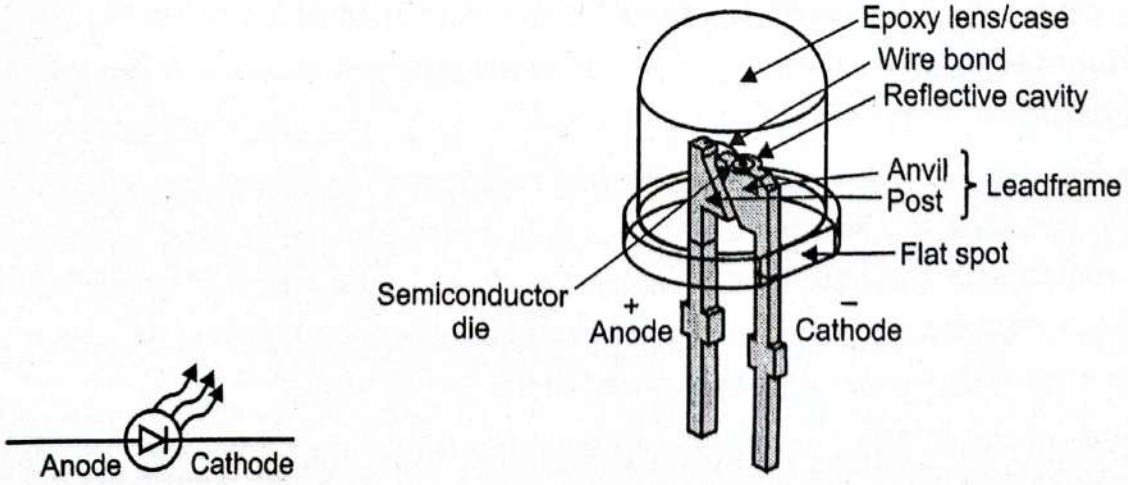


Fig. 2.13: Symbols of LED

Types of LEDs:

By mixing together a variety of semiconductor, metal and gas compounds the following list of LEDs can be produced.

1. Gallium Arsenide (GaAs) – infra-red.
2. Gallium Arsenide Phosphide (GaAsP) – red to infra-red, orange.
3. Aluminium Gallium Arsenide Phosphide (AlGaAsP) – high-brightness red, orange-red, orange and yellow.
4. Gallium Phosphide (GaP) – red, yellow and green.
5. Aluminium Gallium Phosphide (AlGaP) – green.
6. Gallium Nitride (GaN) – green, emerald green.
7. Gallium Indium Nitride (GaInN) – near ultraviolet, bluish-green and blue.
8. Silicon Carbide (SiC) – blue as a substrate.
9. Zinc Selenide (ZnSe) – blue.
10. Aluminium Gallium Nitride (AlGaN) – ultraviolet.

LEDs Working Principle:

LEDs work based on electroluminescence, producing light at forward voltages between 1.8 and 3.6 volts.

The LED structure consists of three semiconductor layers: a P-type region, an N-type region, and an active region where electrons and holes recombine to emit light.

When forward biased, electrons and holes in an LED recombine at the depletion layer, releasing energy as light.

LEDs Construction:

When, an LED is operated in a forward biased direction, it converts electrical energy into light energy. Its construction is very different from that of a normal signal diode. The PN junction of an LED is surrounded by a transparent, hard plastic epoxy resin hemispherical shaped shell or body that protects the LED from both vibration and shock.

Surprisingly, an LED junction does not actually emit that much light so the epoxy resin body is constructed in such a way that the photons of light emitted by the junction are reflected away from the surrounding substrate base to which the diode is attached and are focused upwards through the domed top of the LED, which itself acts like a lens concentrating the amount of light. Hence, the emitted light appears to be brightest at the top of the LED.

However, not all LEDs are made with a hemispherically shaped dome for their epoxy shell. Some indication LEDs have a rectangular or cylindrical shaped construction that has a flat surface on top or their body is shaped into a bar or arrow.

Generally, all LEDs are manufactured with two legs protruding from the bottom of the body. Also, nearly all modern light emitting diodes have their cathode, (–) terminal identified by either a notch or flat spot on the body or by the cathode lead being shorter than the other as the anode (+) lead is longer than cathode (k).

Unlike normal incandescent lamps and bulbs, which generate large amounts of heat when illuminated, the light emitting diode produces a "cold" generation of light, which leads to high efficiencies than normal "light bulbs" because most of the generated energy radiates away within the visible spectrum.

IV Characteristics of LEDs

IV characteristics of Some LEDs are as given below,

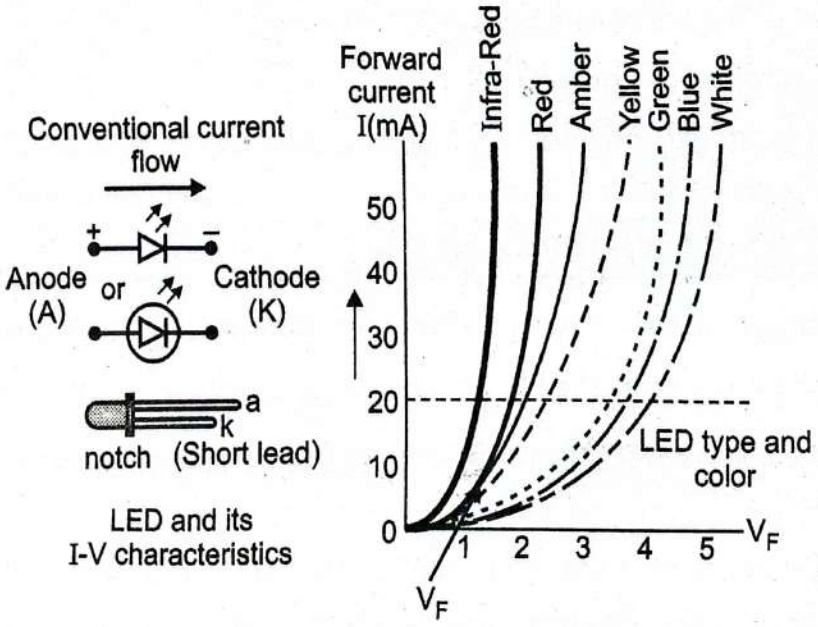


Fig. 2.14: IV characteristics of some LEDs

Advantages of LEDs

- Very fast switching.
- Quite small in size.
- Can be operated with very low voltage.
- A very long life expectancy.
- Construction procedure permits manufacturing in different shapes and patterns.
- LEDs can operated over a wide range of temperature ranging from 0°C – 70°C Economical and Reliable and Portable.
- Higher Efficiency to convert electric energy to light.

Disadvantages of LEDs

- In Overvoltage or Overcurrent.
- In Overheating due to radiant power.

Applications of LEDs

- In Indicator in AC circuit.
- In Display Panel Indicator.
- In Digital Watches, Calculators and Multimeter.
- In Remote Control Systems and Burglar Alarm Systems.
- LEDs are mostly used in numeric displays indicating the numbers 0 through 9.
- LEDs used in display, in digital meters, clocks, calculators, etc.
- LEDs used as a bulb in homes and industries.
- LEDs used in motorcycles and cars.
- LEDs used in mobile phones to display the message.
- LEDs used at traffic light signals.

These are the advantages, disadvantages and applications of light emitting diodes. LED is a significant optoelectronic device. It is also used in optical fibre communication systems.

2.8 APPLICATIONS OF JUNCTION DIODE

There are various applications of PN junction diodes in electronics, some are listed as follows:

- A most common use case of a PN junction diode is as a rectifier to convert AC to DC.
- A Zener diode (It's a special type of PN junction diode) is used in circuits for voltage regulation.
- A Diode only conducts current in forward bias, so in electrical circuits, it is used as a switch to turn on and off certain small circuits in a much more complex circuit.
- A reverse-biased p-n junction diode is utilized as a photodiode as it is sensitive to light.
- LED (It's a special type of PN junction diode) used in a forward basis that emits light.

2.9 NUMERICALS

Problem 2.1: *A silicon diode is subjected to a forward voltage (V) of 0.7V at room temperature (27°C) with a saturation current (I_0) of 10^{-12} A. Calculate the forward current (I) assuming an ideality factor (n) of 1.*

Given Data: Reverse saturation current,

$$I_0 = 10^{-12}\ A$$

Voltage across diode,

$$V_D = 0.7\ V,$$

Ideality factor, $n = 1,$

Temperature, $T = 273 + 27 = 300\ K$

First, calculate thermal voltage V_T.

$$V_T = \frac{KT}{q}$$

where, V_Y = Thermal voltage

K = Boltzman's constant (1.3806×10^{-23} eV/k)

T = Absolute temperature (Kelvin)

q = Charge of an electron (1.602×10^{-19}C)

$$V_T = \frac{KT}{q}$$

$$V_T = \frac{(1.3806 \times 10^{-23} \text{ ev/K}) \times (300 \text{ K})}{1.602 \times 10^{-19}\text{C}}$$

$$V_T = 0.0259 \text{ V} \quad \ldots(1)$$

Used Shockley equation to find current in diode.

$$I = I_o\left(e^{\frac{V}{nV_T}} - 1\right)$$

$$I = 10^{-12}\left(e^{\frac{0.7}{0.0259}} - 1\right)$$

$$I = 10^{-12}\,(e^{27.03} - 1)$$

$$I = 10^{-12}\,(5.32 \times 10^{11} - 1)$$

$$I = 0.532 \text{ A}$$

Therefore, the diode current I is 0.532 A.

QUESTIONS

1. Explain the formation of a diode?
2. What is meant by an unbiased PN junction?
3. What is meant by depletion layer in an unbiased PN junction?
4. Define forward static and dynamic resistances of a diode.
5. State the principle of LED and explain its working.
6. Draw V-I characteristics of PN junction Diode.
7. Write Diode Current equation and explain each term in it.
8. What is meant by LED? What materials are used to construct an LED?
9. Explain IV characteristics of LED.

10. What is a PN junction diode?
11. Why is silicon preferred over Germanium in the manufacture of semiconductor devices?
12. Define forward and reverse recovery time of a diodes.
13. Define knee voltage and breakdown voltage with respect to diode.
14. What is meant by the mean life time of a carrier in semiconductor?
15. Explain the operation of forward biased and reverse biased PN junction diodes.
16. Explain the current components in a PN junction diodes.
17. Derive the diode current equation.

Module - III

IMPORTANT DIODES

Syllabus:

- *Working of photo diode, Solar cell, Zener diode, Varactor diode, Gunn diode and their applications.*

Objectives:

- *To learn about few special diode important for semiconductor industry.*

Outcome:

- *Learners will be able to Plot the IV characteristics and understand their applications of some special diodes.*

List of Contents:

3.1 Introduction

3.2 Photo Diode, its Working and its Applications

3.3 Solar Cell, its Working and its Applications

3.4 Zener Diode, its Working and its Applications

3.5 Varactor Diode, its Working and its Applications

3.6 Gunn Diode, its Working and its Applications

3.7 Numericals

- *Questions*

3.1 INTRODUCTION

A diode is a specialized electronic component that acts as a one-way switch, conducting electric current in only one direction. It restricts current from the opposite direction. In reverse biased when it acts as an insulator. In forward bias when it allows current to flow. It allows current to flow through in one direction only. It is used to secure circuits from over-voltage and to change AC current to DC current.

A PN junction is formed when N-type material is fused together with a P-type material, creating a semiconductor diode. The N-type region has an excess of electrons, while the P-type region has an excess of holes. The interface between these two different types of materials is termed as a PN junction.

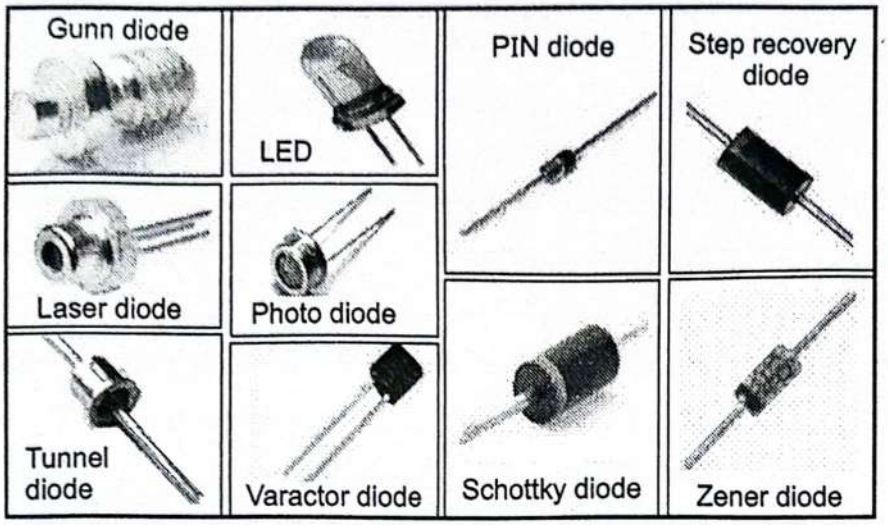


Fig. 3.1: Symbol of some important diodes

3.2 PHOTO DIODE, ITS WORKING AND ITS APPLICATIONS

Photodiodes are special diodes that can detect any light that falls on them. It works in reverse bias conditions and produces current when a certain amount of light energy falls over it. A photodiode is a P-N junction diode that will conduct current when exposed to light. This diode is actually designed to operate in the reverse bias mode. It means that the larger the intensity of falling light, the greater the reverse bias current will be. The following Fig. 3.2 shows a schematic symbol and constructional detail of a photo diode.

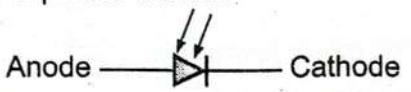


Fig. 3.2: Symbol of photodiode

Types of Photodiode:

Although there are numerous types of photodiode, available in the markets and they all work on the same basic principles, some are improved by other effects. The working of different types of photodiodes works in a slightly different way, but the basic operation of these diodes remains the same. The types of photodiodes can be classified based on their construction and functions as follows:

- PN Photodiode
- Schottky Photodiode
- PIN Photodiode
- Avalanche Photodiode

Principle of Operation:

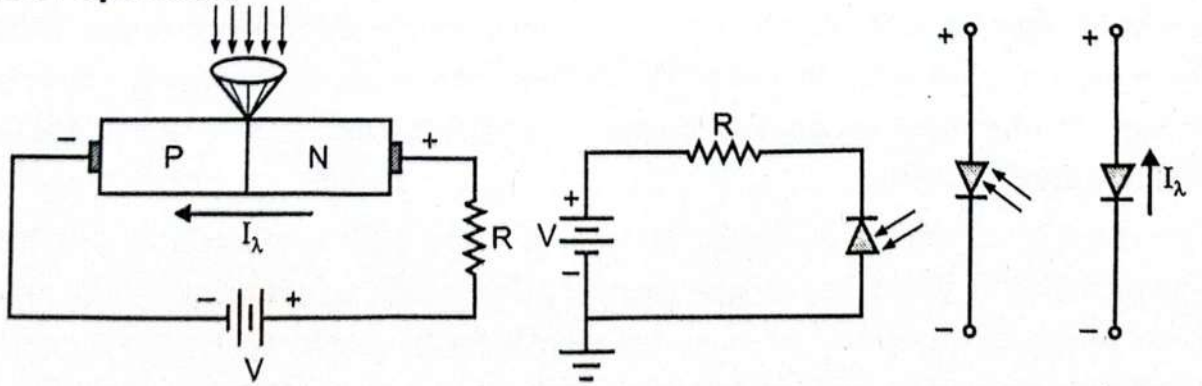


Fig. 3.3: Basic biasing arrangement and construction of photodiode and symbols

A photodiode is a type of photo detector capable of converting light into either current or voltage, depending upon the mode of operation. The common, traditional solar cell used to generate electric energy. Under normal conditions it carries a small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombard the p-n junction and some energy is imparted to the valence electrons. So valence electrons break covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus the total number of minority charge carriers increases and hence reverse current increases.

Working of a Photodiode:

It is a **reverse-biased diode**, reverse current increases as the intensity of incident light increases. This means that reverse current is directly proportional to the intensity of falling light. It consists of a PN junction mounted on a P-type substrate and sealed in a metallic case. The junction point is made of a transparent lens and it is the window where the light is supposed to fall. The reverse current is generated thermally by electron-hole pairs in the depletion region of the diode. When light falls on a PN junction, it is absorbed by the junction. That generates more electron-hole pairs, characteristically reverse current increases.

In other words, as the intensity of falling light increases, the resistance of the PN junction diode decreases.

- This action makes the diode more conductive.
- These diodes have very fast response time.
- These are used in high computing devices.
- It is also used in alarm circuits, counter circuits, etc.

Characteristics of Photodiode:

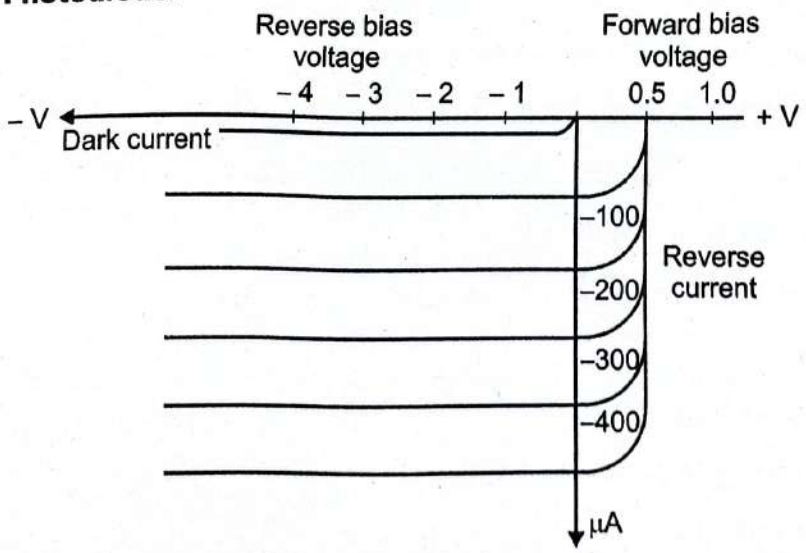


Fig. 3.4: Characteristics of photodiode

When a P-N junction is reverse-biased, a reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as the minority carriers. With the increase in the temperature of the junction more and more hole-electron pairs are created and so

the reverse saturation current I_0 increases. The same effect can be had by illuminating the junction. When light energy bombards a P-N junction, it dislodges valence electrons. The more light striking the junction the larger the reverse current in a diode. It is due to generation of more and more charge carriers with the increase in the level of illumination. This is clearly shown in 'figure for different intensity levels. The dark current is the current that exists when no light is incident.

Operation Modes of Photodiode

The operating modes of the photodiode include three modes, namely Photovoltaic mode, photoconductive mode and avalanche diode mode

- **Photovoltaic Mode:** This mode is also known as zero-bias mode, in which a voltage is produced by the lightened photodiode. It gives a very small dynamic range and non-linear necessity of the voltage formed.
- **Photoconductive Mode:** The photodiode used in this photoconductive mode is more usually reverse biased. The reverse voltage application will increase the depletion layer's width, which in turn decreases the response time and junction capacitance. This mode is too fast and displays electronic noise.
- **Avalanche Diode Mode:** Avalanche diodes operate in a high reverse bias condition, which permits the multiplication of an avalanche breakdown to each photo-produced electron-hole pair. This outcome is an internal gain in the photodiode, which slowly increases the device response.

Advantages of Photodiodes

The advantages of photodiodes include following:

- It is used as a variable resistance device.
- Highly sensitive to the light.
- The speed of operation is very high.
- Less resistance
- Long life span.
- Spectral response is good.
- Frequency response is good.
- Solid and low-weight.
- It is extremely responsive to the light.
- Dark current is less.
- High quantum efficiency.
- Less noise.

Disadvantages of Photodiode

The disadvantages of photodiodes include the following

- Poor temperature stability.
- Temperature dependent dark current.
- Temperature stability is poor.
- Change within current is extremely little, therefore may not be enough to drive the circuit.
- It has less sensitivity.
- It uses offset voltage.

Applications of Photodiode

- Used in consumer electronics devices like smoke detectors, compact disc players, and televisions and remote controls in VCRs.
- Used in other consumer devices like clock radios, camera light meters, and street lights, photoconductors are more frequently used rather than photodiodes.
- Photodiodes are frequently used for exact measurement of intensity of light in science and industry. Generally, they have an enhanced, more linear response than photoconductors.
- It is widely used in numerous medical applications like instruments to analyze samples, detectors for computed tomography, and also used in blood gas monitors.
- It is much faster and more complex than normal PN junction diodes and hence is frequently used for lighting regulation and in optical communications.
- It allows transmission of signals between circuits without a direct metallic connection between them.
- It allows isolation from high voltage differences.
- As photodetectors, they detect optical signals.
- It is used in simple day-to-day applications: Alarm system and counting system.

3.3 SOLAR CELL, ITS WORKING AND ITS APPLICATIONS

A solar cell is an energy conversion device that is used to convert sunlight into electricity by using the photovoltaic effect. It is also known as a photovoltaic cell (PV cell). It is usually made from silicon. A simple solar cell consists of a sandwich of a silicon-boron layer and a silicon–arsenic layer. A basic solar/photovoltaic cell consists of n-type and p-type semiconductors forming a p-n junction. The upper area is extended and transparent, generally exposed to the sunrays. These diodes or cells are exceptional that generate a voltage when exposed to light. This cell converts light energy directly into electrical energy.

Construction of Photovoltaic/Solar Cell:

A very thin layer of p-type semiconductor is grown on a relatively thicker n-type semiconductor. Then apply a few finer electrodes on top of the p-type semiconductor layer. These electrodes do not obstruct light from reaching the thin p-type layer. Just below the p-type layer there is a p-n junction. To provide a current collecting electrode at the bottom of the n-type layer and encapsulate the entire assembly with thin glass to protect the **solar cell** from any mechanical shock.

Working of a Photovoltaic/Solar Cell:

There is no current flow through the device when no light is applied. In this state, the cell will not be able to generate current.

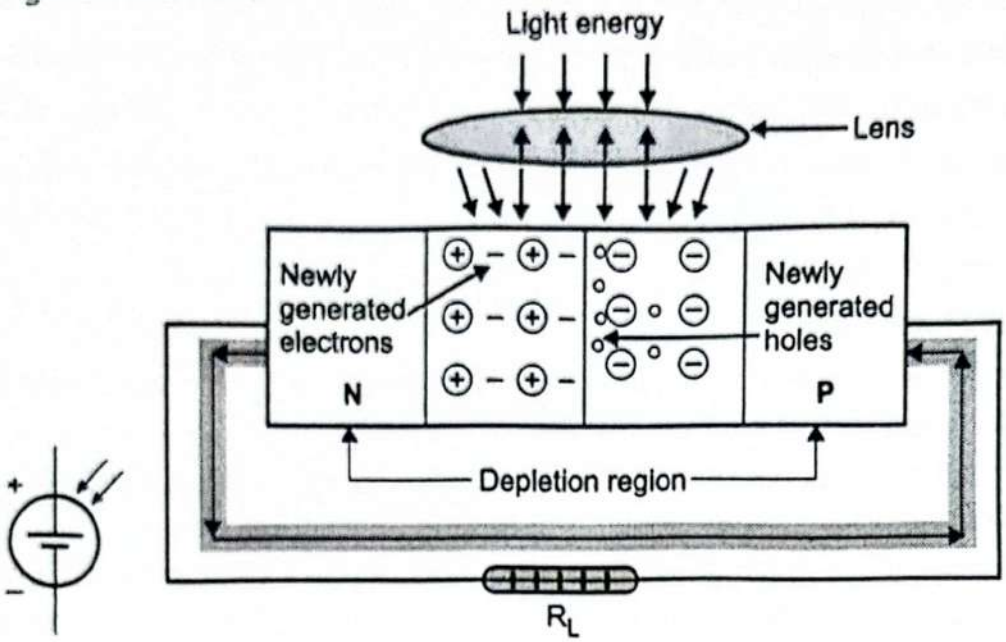


Fig. 3.5: Symbol and reverse biased of photovoltaic/solar Cell

It is essential to bias the cell properly which requires a fair amount of light. As soon as light is applied, a remarkable state of P-N junction diode can be observed. As a result, the electrons acquire sufficient energy and break away from the parent atoms. These newly generated electron-hole pairs in the depletion region cross the junction.

In this action, the electrons move into the N type material because of its normal positive ion concentration. Likewise, holes sweep into the P type material because of its negative ion content. This causes the N type material to instantly take on a negative charge and the P material to take on a positive charge. The P-N junction then delivers a small voltage as a response.

A voltage is set up that is known as photo voltage. If we connect a small load across the junction, there will be a tiny current flowing through it.

Characteristics of a Photovoltaic/Solar Cell:

The following Fig. 3.6, shows one of the characteristics, a graph between reverse current (I_R) and illumination (E) of a photo diode. IR is measured on the vertical axis and illumination is measured on the horizontal axis. The graph is a straight line passing through the zero position.

i.e., $I_R = mE$

Where, m is a slope.

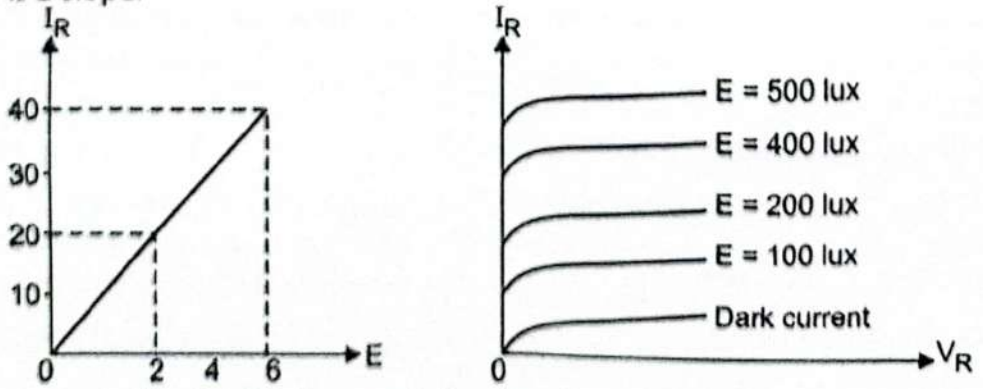


Fig. 3.6: IV characteristics of a photovoltaic/solar cell

Materials Used in Solar Cell

Materials used in solar cells must possess a band gap close to 1.5 eV to optimize light absorption and electrical efficiency. Commonly used materials are

- Silicon
- GaAs
- CdTe
- $CuInSe_2$

Criteria for Materials to be Used in Solar Cell

- Must have a band gap from 1 eV to 1.8 eV.
- It must have high optical absorption.
- It must have high electrical conductivity.
- The raw material must be available in abundance and its cost must be low.

Advantages of Solar Cell

- No pollution associated with it.
- It must last for a long time.
- No maintenance cost.

Disadvantages of Solar Cell

- It has a high cost of installation.
- It has low efficiency.
- During cloudy day, the energy can't be produce and also at night it will not produce the solar energy.

Application/Uses of Solar Cell

Solar cells power devices from small calculators and wristwatches to large-scale applications in spacecraft, highlighting their versatility and growing importance in renewable energy systems.

3.4 ZENER DIODE, ITS WORKING AND ITS APPLICATIONS

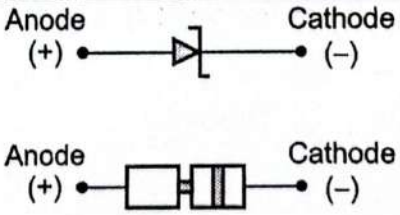


Fig. 3.7: Symbol of zener diode

A Zener diode is like a general-purpose diode consisting of a silicon PN junction. When biased in the forward direction, it behaves just like a normal diode that passed the rated current, but as soon as a reverse voltage is applied across the Zener diode that exceeds the rated voltage of the device, the diode's breakdown voltage is reached, at which point a process called *Avalanche Breakdown* occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

V-I Characteristics of Zener Diode

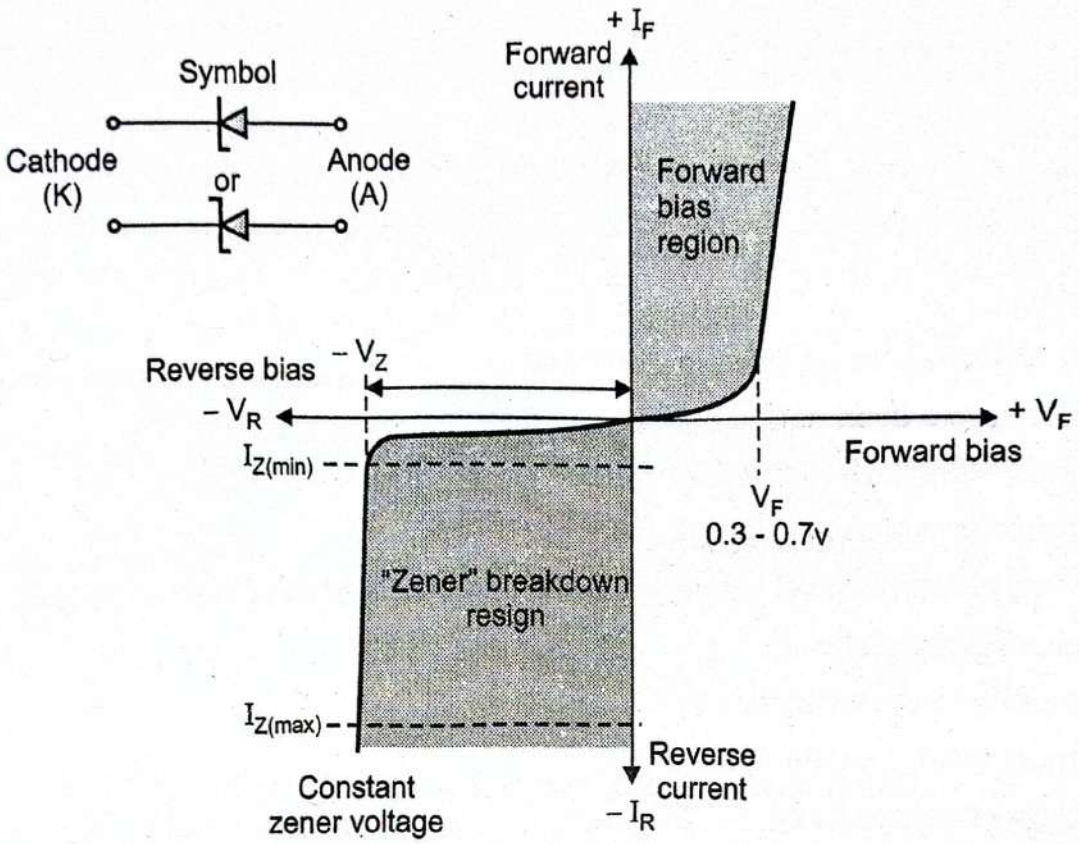


Fig. 3.8: Zener diode VI Characteristics

Forward Characteristics of Zener Diode

Forward characteristics of the Zener diode are similar to the forward characteristics of any normal diode. It is clearly evident from the above diagram (Fig. 3.8) in the first quadrant that the V-I forward characteristics are similar to other P-N junction diodes.

Reverse Characteristics of Zener Diode

In reverse voltage conditions a small amount of current flows through the Zener diode. This current is because of the electrons that are thermally generated in the Zener diode. As we keep increasing the reverse voltage at any particular value of reverse voltage the reverse current increases suddenly at the breakdown point this voltage is called Zener Voltage and is represented as Vz.

Table 3.1

Avalanche Breakdown	Zener Breakdown
• Avalanche breakdown occurs when the high voltage increases the free electron in the semiconductor and a sudden increase in current is seen.	• Zener breakdown happens when electrons from the valence band gain energy and reach the conduction band, which then conducts electricity.
• Avalanche breakdown is seen in the diodes having breakdown voltage greater than 8 volts.	• Zener breakdown is seen in the diodes having breakdown voltage in the range of 5 to 8 volts.

Avalanche Breakdown	Zener Breakdown
• Avalanche breakdown is observed in diodes that are lightly doped.	• Zener breakdown is observed in diodes that are highly doped.
• In Avalanche breakdown, the VI characteristics curve is not as sharp as the VI characteristics curve in Zener breakdown.	• Zener Breakdown has a sharp VI characteristics curve.
• For Avalanche breakdown, an increase in temperature increases the breakdown voltage.	• For Zener breakdown, an increase in temperature decreases the breakdown voltage.

Applications of Zener Diode

A Zener diode is a useful diode. Due to its ability to allow current to flow in reverse bias conditions, it is used widely for various purposes. Uses of Zener Diodes are as follows:

- **Zener Diode as Voltage Regulator:** The Zener diode is utilized as a shunt voltage controller for managing voltage across little loads. The breakdown voltage of Zener diodes will be steady for a wide scope of current. The Zener diode is associated with corresponding to the heap to make it switch predisposition and when the Zener diode surpasses knee voltage, the voltage across the heap will become consistent.
- **Zener Diode in Over-Voltage Protection:** At the point when voltage is higher than the Zener breakage voltage, the voltage across the resistor drops, bringing about a short-out. This can be kept away from by utilizing the Zener diode.
- **Zener Diode in Clipping Circuits:** Zener diodes are utilized for adjusting AC waveform cutting circuits by restricting the pieces of it is possible that one or both of the half patterns of an AC waveform.

Zener Diode Specification

- **Zener Voltage:** The voltage at which Zener breakdown occurs in a Zener diode is called as Zener Voltage. It is denoted by V_z generally, it ranges from 2.4 volts to 200 volts.
- **Current I_z (max):** The maximum current that the diode can achieve at the Zener voltage is called max current. It ranges from 200 μA to 200 A.
- **Current I_z (min):** The minimum current required for the diode to break down is called min current I_z.
- **Power Rating:** Power is calculated by taking the product of breakdown voltage and the value of current at that time.
- **Temperature Stability:** Temperature stability of the Zener diode is greatest at 5V.
- **Voltage Tolerance:** Voltage Tolerance for any Zener diode is normally ±5%.
- **Zener Resistance (R_z):** The resistance exhibited by this diode is a Zener Resistance.

3.5 VARACTOR DIODE, ITS WORKING AND ITS APPLICATIONS

This is a special P-N junction diode with an inconsistent concentration of impurities in its P and N materials. Varactor diode doped with a very small quantity of impurities near the junction and impurity concentration increases moving away from the junction. A Varactor diode is a type of diode whose internal capacitance depends on the reverse voltage. The junction capacitance varies with variation in reverse voltage, and therefore it is also called a varicap diode. These are also called as voltage variable capacitance. It operated in between reverse voltage. This Diode is designed to respond to the capacitance effect under reverse bias, called the voltage variable capacitor.

The capacitance of a Varactor diode is expressed as,

$$C_T = E\frac{A}{W_d}$$

C_T = Total capacitance of the junction
E = Permittivity of the semiconductor material
A = Cross-sectional area of the junction
W_d = Width of the depletion layer

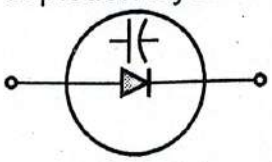
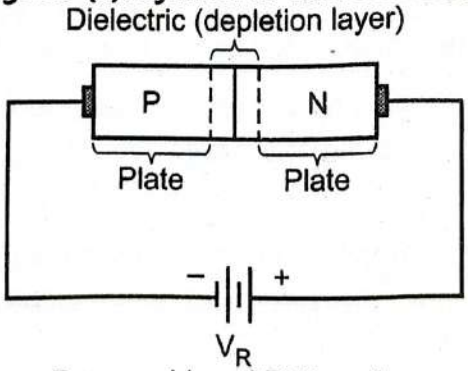


Fig. 3.9 (a): Symbol of Varactor diode



Reverse biased PN junction

Fig 3.9 (b): Reverse biased of varactor diode

If reverse voltage applied is increased, the width of the dielectric region increases, which reduces the junction capacitance. When the reverse voltage decreases, the width of the dielectric decreases, which increases the capacitance. If this reverse voltage is completely null, then the capacitance will be at maximum. In short, as reverse voltage increases, the transition capacitance falls rapidly. This behavior describes an exponential pattern.

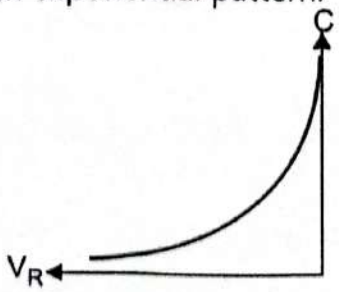


Fig. 3.9 (c): Voltage- capacitance characteristics curve of Varactor diode

This graph shows a non-linear relationship between capacitance and voltage applied to the diode. As we know, capacitance and width have an inverse relationship that means the width of the depletion region increases with reverse voltage and the capacitance decreases (i.e., varies inversely Fig. 3.9 (c)). This nonlinearity allows the varactor to be used also as a harmonic generator.

Advantages of Varactor Diodes

- **Variable Capacitance:** The main advantage of varactor diode is that we can use it as a variable capacitor. Due to this property it can be used as for frequency tuning circuits.
- **Frequency Synthesizer:** Due to the small size of varactor diode and variable capacitance, it can be used in high frequency elements of electronic devices to generate precise frequencies.
- **Phase Shifters:** In PLL (phase-locked loop) circuits, varactor diodes can be used to create voltage-controlled phase shifters, allowing precise phase control.
- **Frequency Multipliers and Dividers:** Varactor diodes are used in frequency multipliers and dividers to generate or divide frequencies as needed.
- **Economically Affordable:** Varactor diodes can be used in tuning circuits at many levels since they are economical and affordable. They also generate less noise as compared to other diodes.

Disadvantages of Varactor Diodes

- **Mode-Specific:** The designing of these diodes is done to operate them in reverse-bias hence they are not useful in forward bias.
- **Non-linear Behavior:** The major drawback of this diode is its non-linear capacitance-voltage relation, which can result in distortion in many appliances.
- **Sensitive:** The capacitance of this diode is largely affected by temperature variations thereby making it temperature-sensitive.

Application of Varactor Diodes

- **Voltage-Controlled Oscillators (VCOs):** Varactor diodes are used in VCOs. VCOs are used in phase-locked loops and communication systems. By varying the voltage across the varactor diode, the capacitance changes which leads to change of frequency in the oscillator.
- **Frequency Modulation Tuning in Radios:** The varactor diodes are also used in the RF circuits. By varying the voltage across the varactor diode we can adjust the resonance frequency of the tuned circuit which we allow the tuning in FM radios. i.e. FM modulators, automatic frequency control devices and television receivers.
- **Phase Shifters:** Varactor diodes are also implemented in phase array antennas. By varying the capacitance in certain part of antenna array can lead to controlling the phase of emitted signal which can be used for beam steering and shaping.
- **Voltage-Controlled Filters:** Varactor diodes are used in voltage controlled bandpass or low pass filters. The cutoff frequency of filter can be adjusted by varying the voltage across the varactor diode.

3.6 GUNN DIODE, ITS WORKING AND ITS APPLICATIONS

A Gunn diode is a diode even though it does not contain any typical P-N diode junction like the other diodes, but it consists of two electrodes. This diode is also called a Transferred Electronic Device. This diode is a negative differential resistance device, which is frequently used as a low-power oscillator to generate microwaves. It consists of only N-type semiconductor in which electrons are the majority charge carriers. To generate short radio waves such as microwaves, it utilizes the Gunn Effect.

Gunn Effect: The Gunn Effect was discovered by John Battiscombe Gunn. It is defined as the generation of microwave power (power with microwave frequencies of around a few GHz) whenever voltage applied to a semiconductor device exceeds the critical or threshold voltage value.

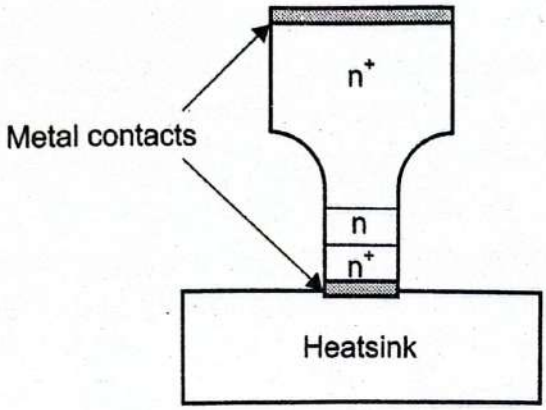


Fig. 3.10 (a): Gunn diode structure

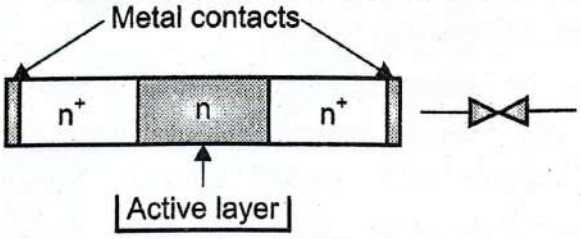


Fig. 3.10 (b): Gunn diode structure and gunn diode symbol

The central region is an active region (Fig. 3.10), which is properly doped N-type GaAs and an epitaxial layer with a thickness of around 8 to 10 micrometers. The active region is sandwiched between the two regions having the Ohmic contacts. A heat sink is provided to avoid overheating and premature failure of the diode and to maintain thermal limits.

For the construction of these diodes, only N-type material is used, which is due to the transferred electron effect being applicable only to N-type materials and is not applicable to the P-type materials. The frequency can be varied by varying the thickness of the active layer while doping.

Working:

This diode is made of a single piece of N-type semiconductor, such as Gallium Arsenide and InP (Indium Phosphide). GaAs and some other semiconductor materials have one band in their electronic band structure instead of having only two energy bands, viz. The valence band and conduction band, like normal semiconductor materials. These GaAs and some other semiconductor materials consist of three energy bands, and this extra third band is empty at the initial stage.

If a voltage is applied to this device, then most of the applied voltage appears across the active region. The electrons from the conduction band, having negligible electrical resistivity are transferred into the third band because these electrons are scattered by applied voltage. The third band of GaAs has mobility that is less than that of the conduction band. Because of this, an increase in forward voltage increases the field strength (for field strengths where applied voltage is greater than threshold voltage value), then the number of electrons reaching the state at which the effective mass increases by decreasing their velocity, and thus the current decreases.

Thus, if the field strength is increased, then drift velocity will decrease, this creates a negative incremental resistance region in the V-I relationship. Thus, an increase in voltage will increase the resistance by creating a slice at the cathode and reaching the anode. But, to maintain a constant voltage, a new slice is created at the cathode. Similarly, if voltage decreases, then the resistance will decrease by extinguishing any existing slice.

Characteristics:

Current-voltage relationship characteristics of a Gunn diode are shown in the above graph with its negative resistance region.

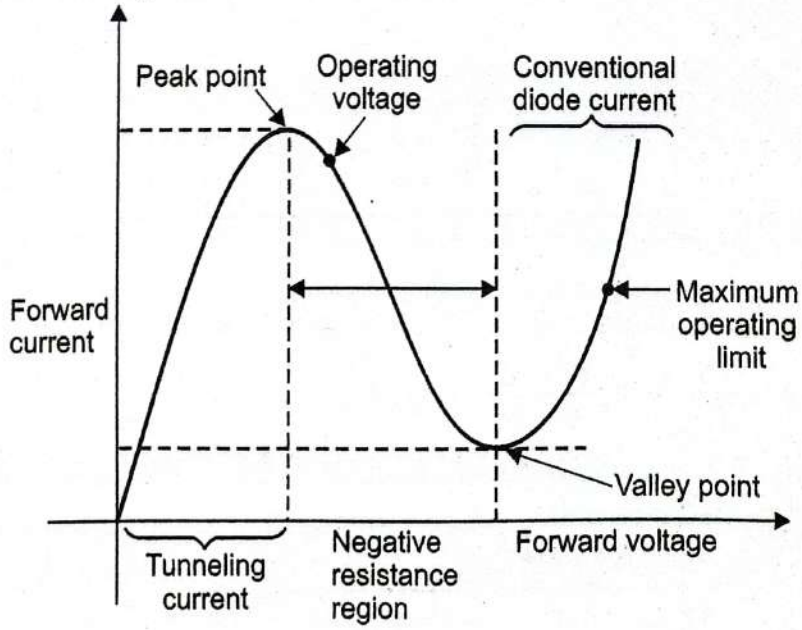


Fig. 3.11: Gunn diode VI characteristics

As shown in the above graph, initially the current increases in this diode, but after reaching a certain voltage level (i.e., threshold value), the current decreases before increasing again. The region where current falls is termed as a negative resistance region, and due to this it oscillates. In this negative resistance region, this diode acts as both an oscillator and an amplifier, as in this region, the diode is enabled to amplify signals.

Applications of Gunn Diode

- Used as Gunn oscillators to generate frequencies ranging from 100 mW (5 GHz) to 1W (35 GHz) outputs. These Gunn oscillators are used in radio communications, military and commercial radar sources.
- Used as sensors for detecting trespassers to avoid derailment of trains.
- Used as efficient microwave generators with a frequency range of up to hundreds of GHz.

- Used for remote vibration detectors and rotational speed measuring tachometers.
- Used as a microwave current generator (Pulsed Gunn Diode Generator).
- Used in microwave transmitters to generate microwaves at very low powers.
- Used as fast controlling components in microelectronics, such as for modulation of semiconductor injection lasers.
- Used as sub-millimeter wave applications by multiplying Gunn oscillator frequency with diode frequency.
- Some other applications include door opening sensors, process control devices, barrier operation, perimeter protection, pedestrian safety systems, linear distance indicators, level sensors, moisture content measurement and intruder alarms.

3.7 NUMERICALS

Problem 3.1: *For the circuit shown find: (i) output voltage (ii) voltage drop across series resistance (iii) current through Zener diode.*

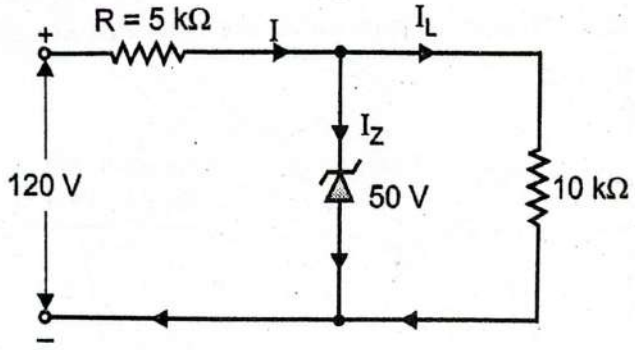


Fig. 3.12

Solution: If we remove Zener diode in Fig. 3.12, the voltage V across the open-circuit is,

$$V = \frac{R_L E_i}{R + R_L} = \frac{10 \times 120}{5 + 10} = 80 \text{ V}$$

Since voltage across Zener diode is greater than VZ (= 50 V), the Zener is in the "on" state. It can, therefore, be represented by a battery of 50 V as shown

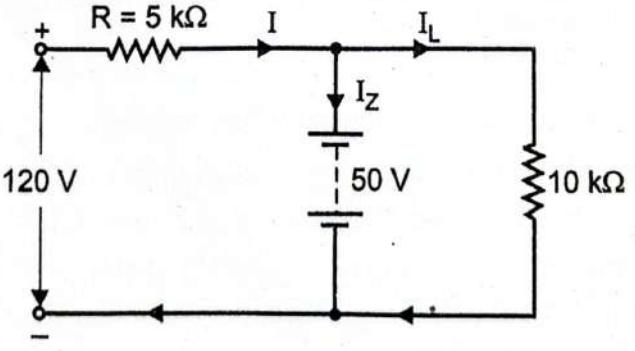


Fig. 3.13

Referring this Fig. 3.13,

Output voltage = V_Z = **50 V**

Voltage drop across R = Input voltage – V_Z = 120 – 50 = **70 V**

Load current, $I_L = \frac{V_Z}{R_L} = \frac{50 \text{ V}}{10 \text{ k}\Omega} = 5 \text{ mA}$

Current through R, $I = \frac{70\ V}{5\ k\Omega} = 14\ mA$

Applying Kirchhoff's first law,

$$I = I_L + I_Z$$

∴ Zener current,

$$I_Z = I - I_L = 14 - 5 = \mathbf{9\ mA}$$

Problem 3.2: *For the circuit shown (i), find maximum and minimum values of Zener current.*

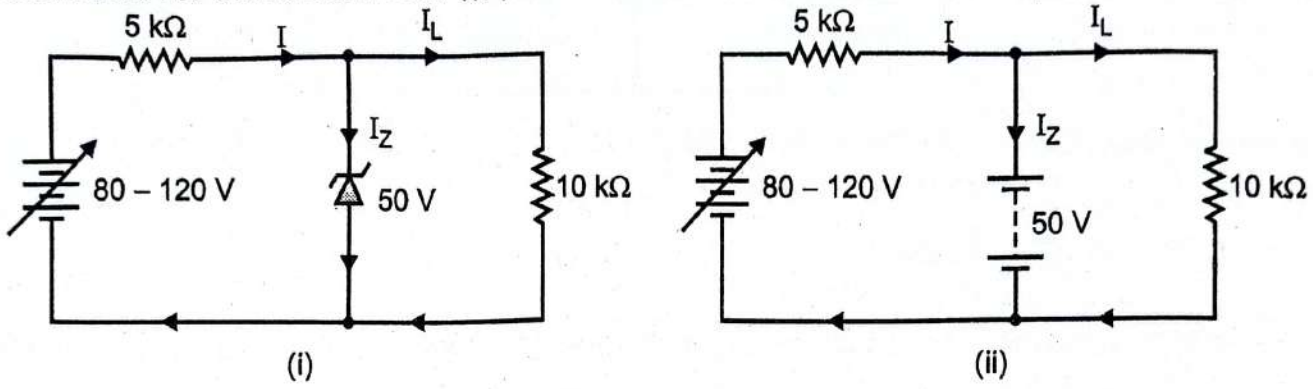


Fig. 3.14

Solution: Voltage Range is 80 – 120 V, the voltage across Zener is greater than the V_Z (= 50V). Hence the Zener diode will be in "on" state for this range of voltages. Consequently, it can replaced by a battery 50 V as shown in Fig. 3.14 (ii).

Maximum Current: Zener conduct maximum current when input voltage is maximum i.e., 120 V. Under such conditions,

Voltage across 5 kΩ = 120 – 50 = 70 V

Current through 5 kΩ,

$$I = \frac{70\ V}{5\ k\Omega} = 14\ mA$$

Load current, $I_L = \frac{50\ V}{10\ k\Omega} = 5\ mA$

Applying Kirchhoff's first law,

$$I = I_L + I_Z$$

∴ Zener current,

$$I_Z = I - I_L = 14 - 5 = \mathbf{9\ mA}$$

Minimum Current: Zener conduct minimum current when the input voltage is minimum i.e., 80 V. Under such conditions,

Voltage across 5 kΩ = 80 – 50 = 30 V

Current through 5 kΩ,

$$I = \frac{30\ V}{5\ k\Omega} = 6\ mA$$

Load current, I_L = 5 mA

∴ Zener current,

$$I_Z = I - I_L = 6 - 5 = \mathbf{1\ mA}$$

Problem 3.3: *A 7.2 V Zener is used in the circuit shown below and the load current is to vary from 12 to 100 mA. Find the value of series resistance R to maintain a voltage of 7.2 V across the load. The input voltage is constant at 12V and the minimum Zener current is 10 mA.*

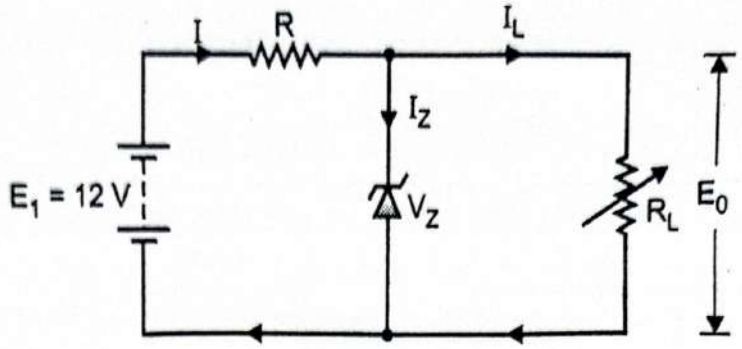


Fig. 3.15

Solution: $E_i = 12\ V;\ V_Z = 7.2\ V$

$$R = \frac{E_i - E_0}{I_Z + I_L}$$

The voltage across R is to remain constant at 12 – 7.2 = 4.8 V as the load current change from 12 to 100 mA. The minimum Zener current will occur when the load current is maximum.

$$\therefore \quad R = \frac{E_i - E_0}{(I_Z)_{min} + (I_L)_{max}} = \frac{12\ V - 7.2\ V}{(10 + 100)\ mA} = \frac{4.8\ V}{110\ mA} = \mathbf{43.5\ \Omega}$$

If R = 43.5 Ω is inserted in the circuit, the output voltage will remain constant over the regulating range. As load current IL decreases, the Zener current will increase to such a value that $I_Z + I_L$ = 110 mA. Note that if the load resistance is open-circuited, then I_L = 0 and Zener current become 110 mA.

QUESTIONS

1. Explain the working of a Photodiodes.
2. State applications of Photodiodes.
3. Explain VI Characteristics of Photodiodes.
4. Explain the working of a solar cell Range.
5. Explain VI Characteristics of Solar Cells.
6. Draw V-I characteristics of a Zener Diode.
7. List the applications of Zener Diodes.
8. Explain the working of a Zener diode and state its applications.
9. Explain the characteristics of a Varactor diode.
10. Explain the working of a Gunn diode and state its applications.

Module - IV

BIPOLAR JUNCTION TRANSISTORS

Syllabus:

- *BJT structure and operation: BJT structure, Modes of operation, CB, CE. I-V characteristics, BJT amplification and switching - current gain, BJT as a switch.*

Objectives:

- *To understand the basics of transistors and their applications in the field of electronics.*

Outcome:

- *Learners will be able to Calculate current gain and Plot I-V characteristics for CB- CE configurations.*

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4.2 BJTs Structures and Operation
4.3 Operation Modes of BJT
4.4 Characteristics of BJT
  4.4.1 Characteristics Curves of Transistor in CB Configuration
  4.4.2 Characteristics Curves of Transistor in CE Configuration
  4.4.3 Characteristics Curves of Transistor in CC Configuration
4.5 Amplification of BJT
  4.5.1 CB Mode Amplification and Current Gain
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4.6 Switching of BJT
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- Questions

4.1 INTRODUCTION

The transistor was invented by a team of three men at Bell Laboratories in 1947. Although this first transistor was not a bipolar junction device, it was the beginning of a technological revolution that is still continuing. All of the complex electronic devices and systems today are an outgrowth of early developments in semiconductor transistors. Two basic types of transistors are the Bipolar Junction Transistor (BJT) and the Field-Effect Transistor (FET). The BJT is used in two broad areas: as a linear amplifier to amplify an electrical signal and as an electronic switch.

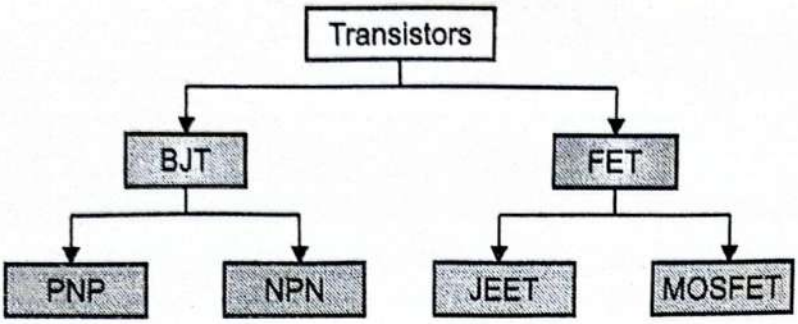

Fig. 4.1: Classification of transistors

Bipolar Junction Transistor:

A Bipolar Junction Transistor (BJT) consists of two p–n junctions with three terminals. BJT is a bipolar device, which means that it is made using p-type and n-type materials as the main substrate. Hence the current conduction in a BJT is done by both electrons and holes.

A BJT is a three terminal electronic device that amplifies the flow of current. It is a current controlled device. The term bipolar refers to the use of both holes and electrons as current carriers in transistor structure. BJT is constructed with three doped semiconductor layers. These are alternating p, n and p layers of a device called a PNP type BJT while n, p and n layers of a device called the NPN type BJT, shown in an epitaxial planer structure in Fig. 4.2 (a). In a transistor, the amplification is achieved by passing input current from a region of low resistance to a region of high resistance.

Transistor can be constructed by various techniques. Based on these, they are classified as:

- Grown junction transistor
- Alloy junction transistor
- Diffusion junction transistor
- Epitaxial junction transistor
- Point contact junction transistor

Applications of BJTs

- In Televisions, Mobile phones, Computers, Radio transmitters and Audio amplifiers.
- BJT is often used in logic and clipping circuits.
- BJT is used as a demodulator and used a detector
- BJT used in temperature sensors
- BJT used as an oscillator.
- BJT as a switch.

Advantages of BJT

- Voltage gain is high.
- It includes maximum current density.
- It provides good performance at high frequency.
- It has a high gain bandwidth.
- High-frequency operation.
- Forward voltage drop is low.
- It operates in low power or high power applications.

Disadvantages of BJT

- Less switching frequency.
- Noise production is more.
- Thermal stability is less.
- Switching Time not as fast as compared to high frequency of voltage and current.

Functions of BJT

- Amplification, Switching and Signal Modulation

4.2 BJT STRUCTURES AND OPERATION

NPN Transistor: When a single p-type semiconductor layer is sandwiched between two n-type semiconductor layers, the transistor is said to be an NPN transistor.

PNP Transistor: When a single n-type semiconductor layer is sandwiched between two p-type semiconductor layers, the transistor is said to be a PNP transistor.

The physical representations of NPN and PNP transistors are shown in Fig. 4.2 (b) and 4.2 (c). The p-n junction joining the base region and emitter region is called the base-emitter junction, while the base region and collector region are called the base-collector junction, as indicated in Fig. 4.2 (b).

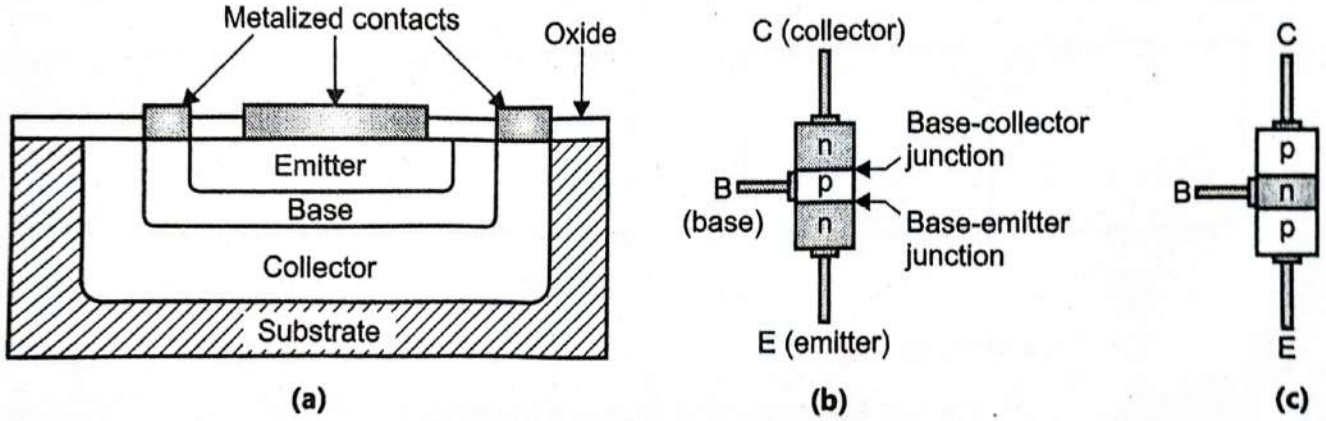

Fig. 4.2: Planar structure of BJT and representations of NPN and PNP structure

A wire lead connects to each of the three regions, as shown that are labeled as E, B and C for emitter, base and collector, respectively. Fig. 4.3 shows the symbols of BJTs.

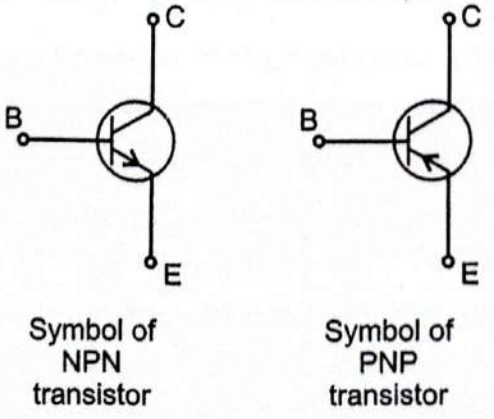

Fig. 4.3: Symbols of NPN and PNP type BJT

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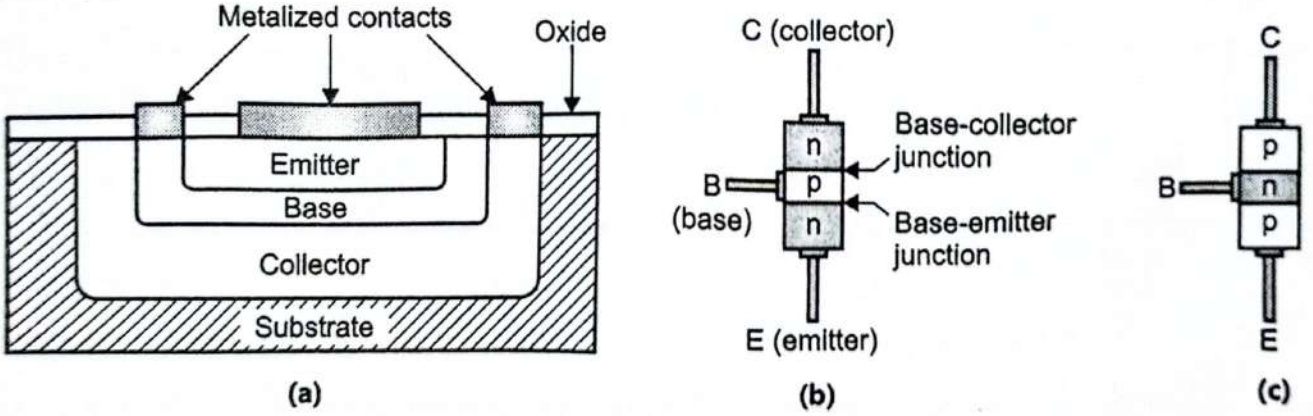

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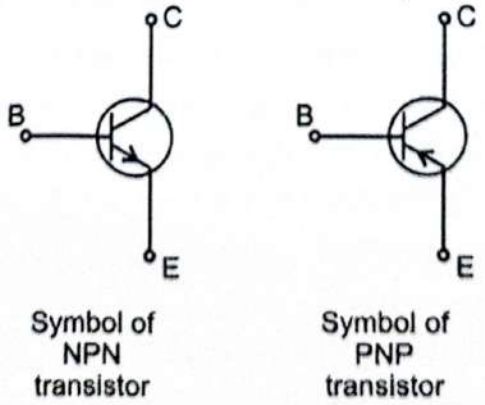
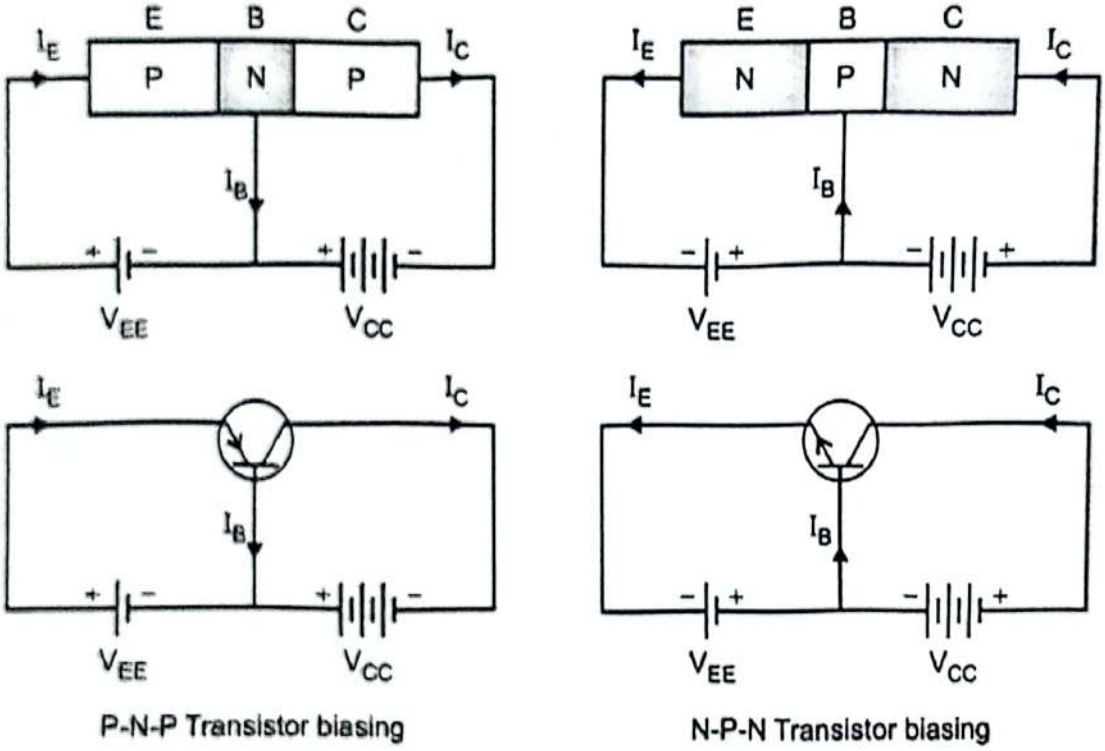


Fig. 4.3: Symbols of NPN and PNP type BJT

Emitter: As the name suggests, the emitter supplies the charge carriers. The emitter section is heavily doped so that it can inject a large number of charge carriers into the base. The size of the emitter is always greater than the size of the base.

Base: The middle layer is called base. The base of the transistor is very thin as compared to the emitter and collector. It is very lightly doped.

Collector: The function of a collector is to collect charge carriers. It is moderately doped. That is the doping level of the collector lies in between the emitter and base. The size of the collector is always greater than the emitter and base. Of course, collector area in transistor is considerably larger than the emitter area.



P-N-P Transistor biasing N-P-N Transistor biasing

Fig. 4.4: Biased of NPN and PNP transistors

1. Operation of PNP Transistor:

The operation of a PNP transistor are explained using the above Fig. 4.4, in which emitter-base junction is forward biased and collector-base junction is reverse biased.

The Forward Biased voltage (V_{EE}) provides a positive potential at the emitter, which repels the holes in P-type material and these holes cross the emitter-base junction to reach the base region. There is a very low percent of holes recombining with free electrons of the N-region. This provides very low current, which constitutes the base current (I_B). The remaining holes cross the collector-base junction to constitute collector current (I_C), which is the hole current.

As a hole reaches the collector terminal, an electron from the battery negative terminal fills the space in the collector. This flow slowly increases and the electron minority current flows through the emitter, where each electron entering the positive terminal of V_{EE}, is replaced by a hole by moving towards the emitter junction. This constitutes emitter current (I_E).

2. Operation of NPN Transistor:

The operation of an NPN transistor is explained using the above the Fig. 4.4, in which the emitter-base junction is forward biased and the collector-base junction is reverse biased. The Forward Biased Voltage (V_{EE}) provides a negative potential at the emitter, which repels the electrons in N-type material and these electrons cross emitter-base junction, to reach the base region.

There is a very low percent of electrons recombining with free holes of the P-region. This provides very low current, which constitutes base current (I_B). The remaining holes cross the collector-base junction to constitute collector current (I_C).

As an electron reaches out of the collector terminal and enters the positive terminal of the battery, an electron from the negative terminal of battery (V_{EE}) enters the emitter region. This flow slowly increases and the electron current flows through the transistor.

4.3 OPERATION MODES OF BJT

In order to operate the transistor, we need to supply dc voltage to the transistor (NPN or PNP). Based on the polarity of the applied dc voltage, the transistors are biased as shown in the below Fig. 4.5. Applying dc voltage to BJTs is nothing but the biasing of the transistor. The supply of suitable external dc voltage is called as **biasing**.

By applying power, ***the emitter base junction is always forward biased while collector base junction is reverse biased.*** These biasing make the BJTs work in three modes of regions such as Active region, Saturation region and Cutoff region.

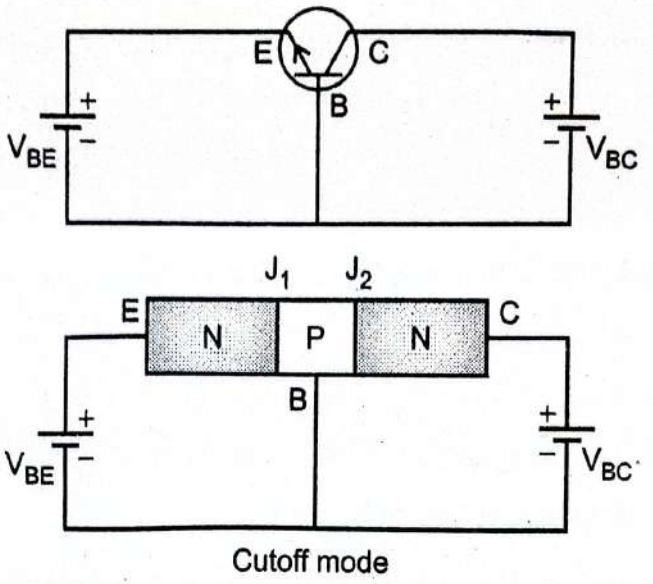
Table 4.1

Emitter Junction	Collector Junction	Region of Operation
Reverse biased	Reverse biased	Cutoff region
Forward biased	Forward biased	Saturation region
Forward biased	Reverse biased	Active region

Cutoff Mode:

In cutoff mode, both the junctions of transistor (emitter to base and collector to base) are reverse biased. In other words, if we assume two p-n junctions as two p-n junction diodes, both the diodes are reverse biased in cutoff mode.

We know that in reverse bias condition, no current flows through the device. Hence, no current flows through transistor. Therefore, the transistor is in off state and acts like an open switch. The cutoff mode of the transistor is used in switching operation for switch OFF application.



Cutoff mode

Fig. 4.5: Schematic of cutoff mode of BJT operation

$I_C = I_E = I_B = 0$

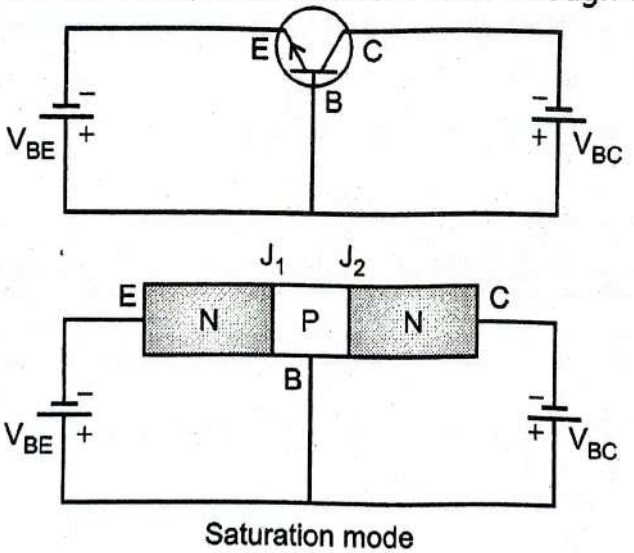
Where, I_C = collector current

I_E = emitter current

and, I_B = base current

Saturation Mode:

In saturation mode, both the junctions of the transistor (emitter to base and collector to base) are forward biased. In other words, if we assume two p-n junctions as two p-n junction diodes, both the diodes are forward biased in saturation mode. We know in forward bias condition, current flows through the device. Hence, electric current flows through the transistor.



Saturation mode

Fig. 4.6: Schematic of saturation mode of BJT operation

In saturation mode, free electrons (charge carriers) flows from emitter to base as well as from collector to base. As a result, a huge current will flow to the base of transistor.

i.e. $I_C = I_E$

Where, I_C = collector current

and I_E = emitter current

Therefore, the transistor in saturation mode will be in an on state and act like a closed switch. This mode of transistor is used in switching operation for switch ON application.

Active Mode:

In active mode, one junction (emitter to base) is forward biased and the other junction (collector to base) is reverse biased. A transistor operates well in the active region and hence it is also called the **Linear Region.** This mode of operation is used for amplification of current. A transistor acts better as an **Amplifier** in this region. This region lies between saturation and cutoff.

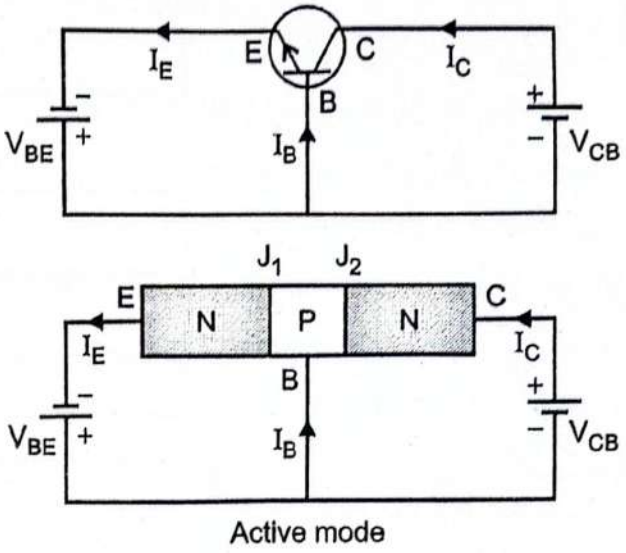
In active state, collector current is β times the base current,

i.e., $I_C = \beta I_B$

Where, I_C = collector current

β = current amplification factor

I_B = base current



Active mode

Fig. 4.7: Schematic of active mode of BJT operation

From these mode of operations, we can say that transistor works as an ON/OFF switch in saturation and cutoff modes whereas it works as an amplifier of current in active mode.

4.4 CHARACTERISTICS OF BJT

4.4.1 Characteristics Curves of Transistor in CB Configuration

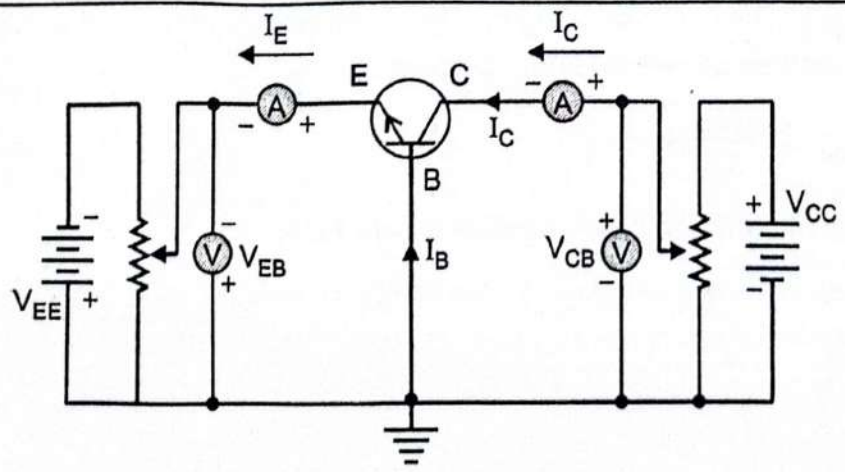


Fig. 4.8: NPN transistor in CB mode

Input Characteristics: The curve plotted between emitter-base voltage (V_{EB}) and emitter current (I_E) keeping collector-base voltage (V_{CB}) constant, is known as the input characteristics of CB transistor. Input characteristics of a CB transistor at constant V_{CB}.

Dynamic Input Resistance(R_{in}): It is defined as the ratio of change in input voltage or emitter voltage (V_{BE}) to the corresponding change in input current or emitter current (I_E), with the output voltage or collector voltage (V_{CB}) kept constant.

$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E}$$

The input resistance of a common base amplifier is very low.

The input and output characteristics of BJT in CB configuration are shown in the below Fig. 4.9.

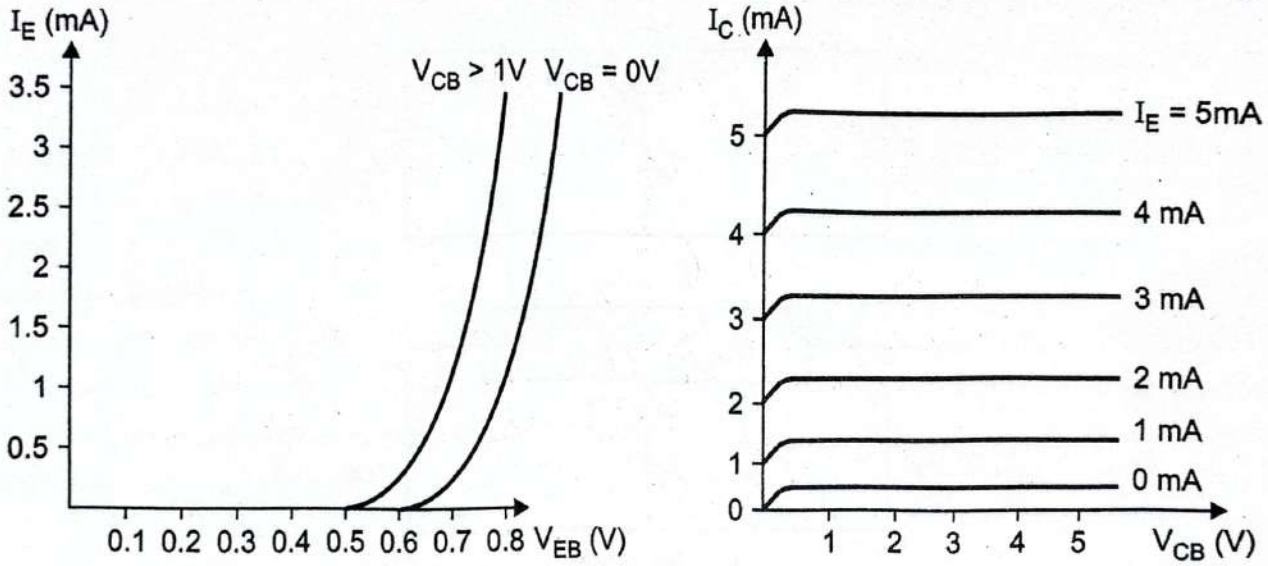


Fig. 4.9: CB mode BJT (a) Input characteristics and (b) Output characteristics

Output Characteristics: The curve plotted between collector current and collector-base voltage (V_{CB}), for a given value of emitter current (I_E) is known as the output characteristics of a CB transistor. Output characteristics of CB transistor at constant I_E.

Dynamic Output Resistance (R_{out}): It is defined as the ratio of change in output voltage or collector voltage (V_{CB}) to the corresponding change in output current or collector current (I_C), with the input current or emitter current (I_E) kept constant.

$$R_{out} = \frac{\Delta V_{CB}}{\Delta I_C}$$

Output resistance of common base amplifier is very high.

Current Gain (α): The current gain of transistor is defined as ratio of output current or collector current (I_C) to the input current or emitter current (I_E), at constant V_{CB}.

$$\alpha = \frac{I_C}{I_E} \text{ at constant } V_{CB}$$

In CB mode, current gain is less than unity. Typically it is 0.98 for common base amplifier.

4.4.2 Characteristics Curves of Transistor in CE Configuration

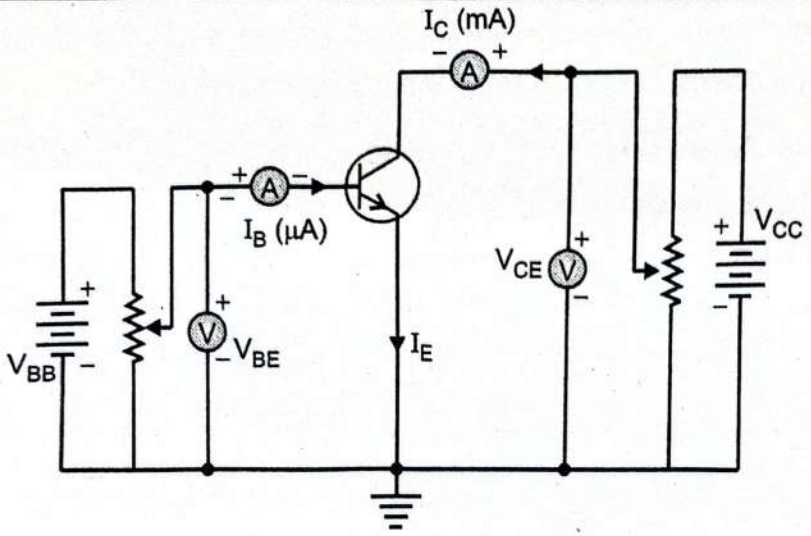


Fig. 4.10: NPN transistor in CE mode

Input Characteristics: The curve plotted between emitter-base voltage (V_{EB}) and emitter current (I_E) keeping collector-base voltage (V_{CB}) constant is known as the input characteristics of CE transistor. Input characteristics of a CE transistor at constant V_{CB}.

Dynamic Input Resistance (R_{in}): It is defined as the ratio of change in input voltage or base voltage (V_{BE}) to the corresponding change in input current or base current (I_B), with the output voltage or collector voltage (V_{CE}) kept constant.

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B}$$

In CE configuration, the input resistance is very low.

The input and output characteristics of BJT in CE configuration are shown in below Fig. 4.11:

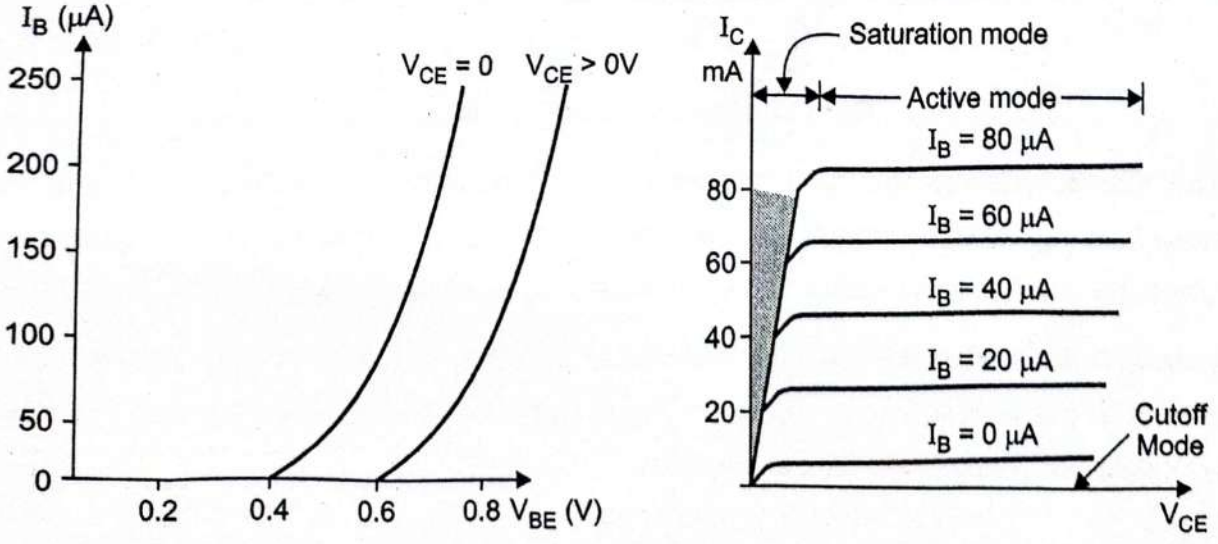


Fig. 4.11: CE mode BJT (a) Input characteristics and (b) Output characteristics

Output Characteristics: The curve plotted between collector current (I_C) and collector-base voltage (V_{CE}), for a given value of emitter current (I_B) is known as the output characteristics of a CE transistor. Output characteristics of CE transistor at constant I_B.

Dynamic Output Resistance (R_o): It is defined as the ratio of change in output voltage or collector voltage (V_{CE}) to the corresponding change in output current or collector current (I_C), with the input current or base current (I_B) kept constant.

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

In a common emitter amplifier output resistance is high.

Current Gain (β): The current gain of a transistor is defined as the ratio of output current or collector current (I_C) to input current or base current (I_B).

$$\beta = \frac{I_C}{I_B}$$

In CE mode, current gain is high. Therefore, a transistor is used for amplifying current.

4.4.3 Characteristics Curves of Transistor in CC Configuration

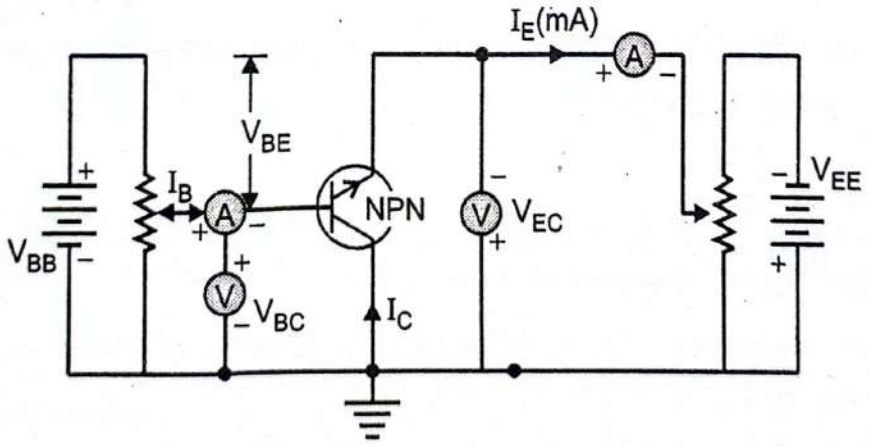


Fig. 4.12: NPN transistor in CC Mode

Input Characteristics: The curve plotted between base-collector voltage (V_{BC}) and base current (I_B) keeping collector-emitter voltage (V_{CE}) constant, is known as the input characteristics of CC transistor. Input characteristics of a CC transistor at constant V_{EC}.

Dynamic Input Resistance (R_{in}): It is defined as the ratio of change in input voltage or base voltage (V_{EB}) to the corresponding change in input current or base current (I_B), with the output voltage or collector voltage (V_{CE}) kept at constant.

$$R_{in} = \frac{\Delta V_{BC}}{\Delta I_B}$$

The input and output characteristics of BJT in CC configuration are shown in below Fig. 4.13:

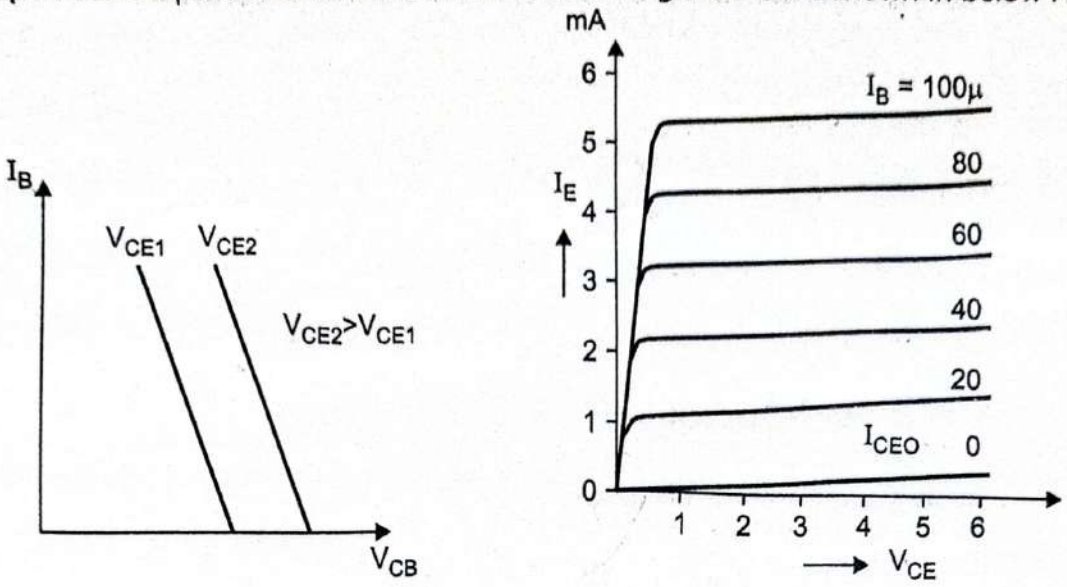


Fig. 4.13: CC mode BJT (a) Input characteristics and (b) Output characteristics

Output Characteristics: The curve plotted between emitter current (I_E) and emitter collector voltage (V_{EC}), for a given value of base current (I_B) is known as the output characteristics of CC transistor. Output characteristics of a CC transistor at constant I_B.

Dynamic Output Resistance (R_o): It is defined as the ratio of change in output voltage or emitter collector voltage (V_{EC}) to the corresponding change in output current or emitter current (I_E), with the input current or base current (I_B) kept constant.

$$R_o = \frac{\Delta V_{EC}}{\Delta I_E}$$

Current Gain (γ): The current gain of a transistor is defined as the ratio of output current or emitter current (I_E) to input current or base current (I_B).

$$\gamma = \frac{I_E}{I_B}$$

In CC mode, the current gain of a transistor is high.

Table 4.2: Comparison of Transistors Configuration Characteristics

Characteristics of Transistor	Common Base	Common Emitter	Common Collector
Power Gain	Low	Very high	Medium
Voltage gain	High	Medium	Low
Amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
Current gain	Low	Medium	High
Phase angle	0	180	0
Output impedance	Very high	High	Low
Input impedance	Low	Medium	High

4.5 AMPLIFICATION OF BJT

A Transistor has 3 terminals, viz. emitter, base and collector. Using three terminals the transistor can be connected in a circuit with one common terminal to both input and output in 3 possible configurations as.

- Common base configuration
- Common emitter configuration
- Common collector configuration

For each mode, the emitter junction is forward biased and the collector junction is reverse biased.

4.5.1 Common Base Mode Amplification and Current Gain

As the name implies that ***Base terminal*** is taken as the common terminal for both input and output of transistor. The common base connection for both NPN and PNP transistors are as shown in the below Fig. 4.14.

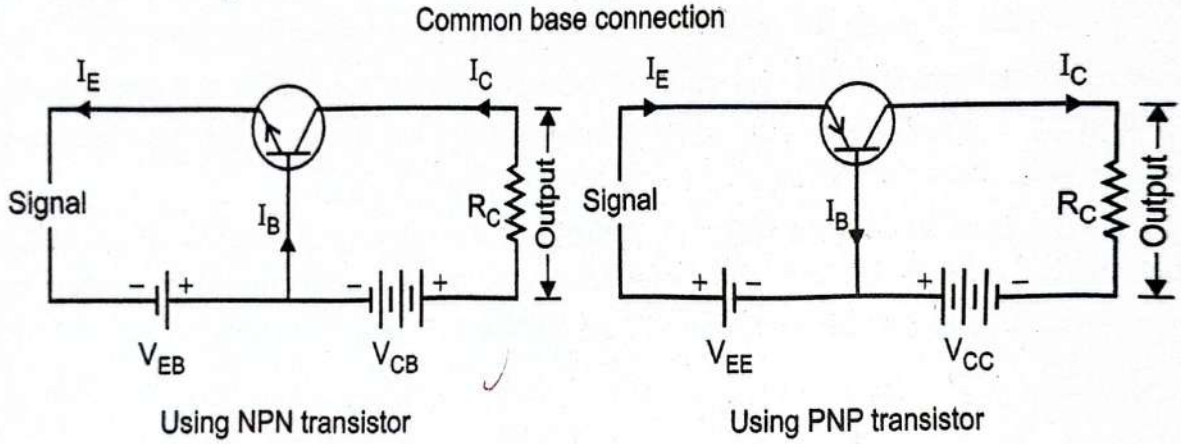


Fig. 4.14: NPN transistor and PNP transistor as CB amplifier

Consider an NPN transistor in CB configuration. When the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons and current flows through the emitter and base to the collector to contribute collector current. The collector voltage (V_{CB}) is kept constant throughout this. In CB configuration, input current is emitter current (I_E) and output current is collector current (I_C).

Current Amplification Factor (α):

The ratio of change in collector current to change in emitter current when collector voltage (V_{CB}) is kept constant, is called the Current amplification factor. It is denoted by α.

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Expression for Collector Current (I_C):

In Common base configuration, as emitter current flows, there is some amount of base current IB that flows through the base terminal due to electron hole recombination. As the collector-base junction is reverse biased, there is another current that is flown due to minority charge carriers. This is the leakage current that we understood as $I_{leakage}$. This current is due to minority charge carriers and hence it is very small.

The emitter current that reaches the collector terminal is αI_E

Then, the total collector current is,

$$I_C = \alpha I_E + I_{leakage}$$

If the emitter-base voltage $V_{EB} = 0$, even then, there flows a small leakage current, which can be termed as I_{CBO} collector base current with the output open.

Therefore, collector current is expressed as,

$$I_C = \alpha I_E + I_{CBO}$$

We know, $I_E = I_C + I_B$

Put the value of I_E then in the previous equation,

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

Then $$I_C = \left[\frac{\alpha}{(1-\alpha)}\right] I_B + \left[\frac{1}{(1-\alpha)}\right] I_{CBO}$$

Hence the above derived expression is for the collector current. It depends on base current and leakage current along with the current amplification factor of the transistor in use.

Characteristics of CB Configuration (Refer Fig. 4.9)

- This configuration provides voltage gain but no current gain.
- Being V_{CB} constant, with a small increase in Emitter-base voltage (V_{EB}), Emitter current I_E gets increased.
- Emitter Current (I_E) is independent of Collector voltage (V_{CB}).
- Collector Voltage (V_{CB}) can affect the collector current (I_C) only at low voltages, when V_{EB} is kept constant.
- The input resistance R_{in} is the ratio of change in emitter-base voltage (ΔV_{EB}) to the change in emitter current (ΔI_E) at constant collector base voltage (V_{CB}).

$$R_{in} = \frac{\Delta V_{EB}}{\Delta I_E} \text{ at constant } V_{CB}$$

- As the input resistance is of very low value, a small value of V_{EB} is enough to produce a large current flow of input current (I_E).
- The output resistance Ro is the ratio of change in collector base voltage (ΔV_{CB}) to change in collector current (ΔI_C) at constant emitter current (I_E).

$$R_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

- As the output resistance is of very high value, a large change in V_{CB} produces a very little change in collector current (I_C).
- This Configuration provides good stability against increase in temperature.
- The CB configuration is used for high frequency applications.

The working principle of a PNP transistor is the same as in an NPN transistor with a CB configuration. But the only difference in NPN transistor is the free electrons conduct the most of the current whereas in PNP transistor the holes conduct the most of the current.

4.5.2 Common Emitter Mode Amplification and Current Gain

As name implies that ***Emitter terminal*** is taken as the common terminal for both the input and output of the transistor. The common emitter connection for both NPN and PNP transistors are as shown in below Fig. 4.15.

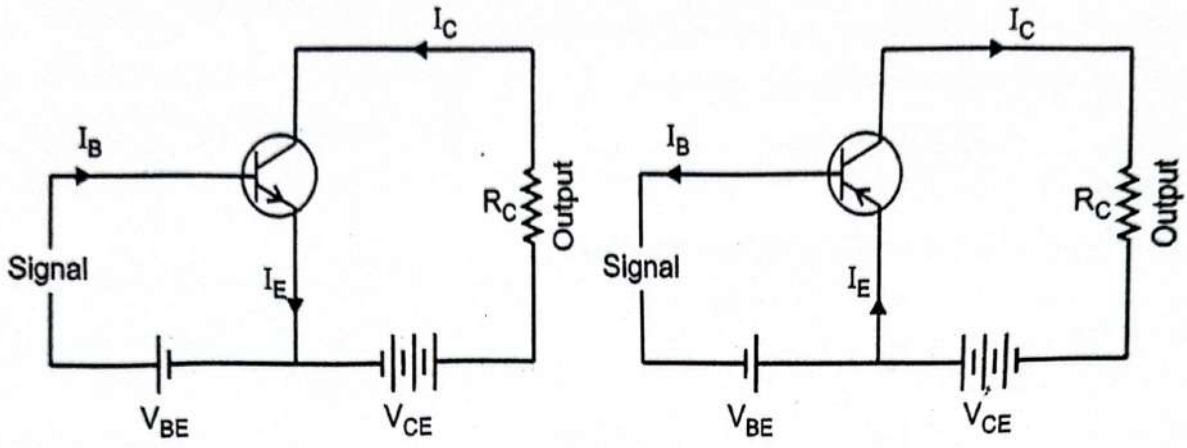


Fig. 4.15: NPN transistor and PNP transistor as CE amplifier

Just as in CB configuration, the emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. The input current is base current I_B and output current is collector current I_C.

Base Current Amplification Factor (β):

The ratio of change in collector current to change in base current is known as the *Base Current Amplification Factor*. It is denoted by β.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relation between β and α:

The relation between base current amplification factor (β) and emitter current amplification factor (α).

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

and

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Then base current amplification factor (β) is

$$\beta = \frac{\Delta I_C}{(\Delta I_E - \Delta I_C)}$$

Dividing by (ΔI_E) to Numerator and Denominator, then

$$\beta = \frac{\left[\frac{\Delta I_C}{\Delta I_E}\right]}{\left[\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}\right]}$$

By using definition of emitter current amplification factor (α)

$$\beta = \frac{\alpha}{(1-\alpha)}$$

This equation represents the relation between β and α. From this, it is evident that, as α approaches 1, β reaches infinity. Hence, current gain in a Common Emitter connection is very high. That's why this circuit connection is mostly used in all transistor applications.

Expression for Collector Current (I_C):

In CE configuration, I_B is input current and I_C is output current.

We know, $I_E = I_B + I_C$

and $I_C = \alpha I_E + I_{CBO}$

Put value of I_E,

Then $I_C = \alpha (I_B + I_C) + I_{CBO}$

$I_C (1-\alpha) = \alpha I_B + I_{CBO}$

Then $$I_C = \left[\frac{\alpha}{(1-\alpha)}\right] I_B + \left[\frac{1}{(1-\alpha)}\right] I_{CBO}$$

If the base circuit is open, i.e., if $I_B = 0$,

The collector emitter current with the base open is I_{CEO}

$$I_{CEO} = \left[\frac{1}{(1-\alpha)}\right] I_{CBO}$$

Substituting this value in the previous equation, we get

$$I_C = \left[\frac{\alpha}{(1-\alpha)}\right] I_B + I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

This is the equation for collector current in CE mode.

Knee Voltage:

In CE configuration, by keeping base current (I_B) constant, if V_{CE} is varied, I_C increases nearly to 1v of V_{CE} and stays constant thereafter. This value of V_{CE} up to which collector current I_C changes with V_{CE} is called the *Knee Voltage*. The transistors, while operating in CE configuration, they are operated above this knee voltage.

Characteristics of CE Configuration (Refer Fig. 4.11)

- This configuration provides good current gain and voltage gain.
- Keeping V_{CE} constant, with a small increase in V_{BE} the base current I_B increases more rapidly than in CB configurations.
- For any value of V_{CE} above knee voltage, I_C is approximately equal to βI_B.
- The input resistance R_{in} is the ratio of change in base emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant collector emitter voltage (V_{CE}).

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

- As the input resistance is of very low value, a small value of V_{BE} is enough to produce a large current flow of base current I_B.
- The output resistance R_o is the ratio of change in collector emitter voltage (ΔV_{CE}) to change in collector current (ΔI_C) at constant I_B.

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

- As the output resistance of CE circuit is less than that of CB circuit.
- This mode is used for bias stabilization methods and audio frequency applications.

4.5.3 Common Collector Mode Amplification and Current Gain

As name implies that **Collector terminal** is taken as the common terminal for both input and output of the transistor. The common collector connection for both NPN and PNP transistors are as shown in the below Fig. 4.16. The emitter junction is forward biased and the collector junction is reverse biased. The flow of electrons is controlled in the same manner. Input current is base current (I_B) and output current is emitter current (I_E).

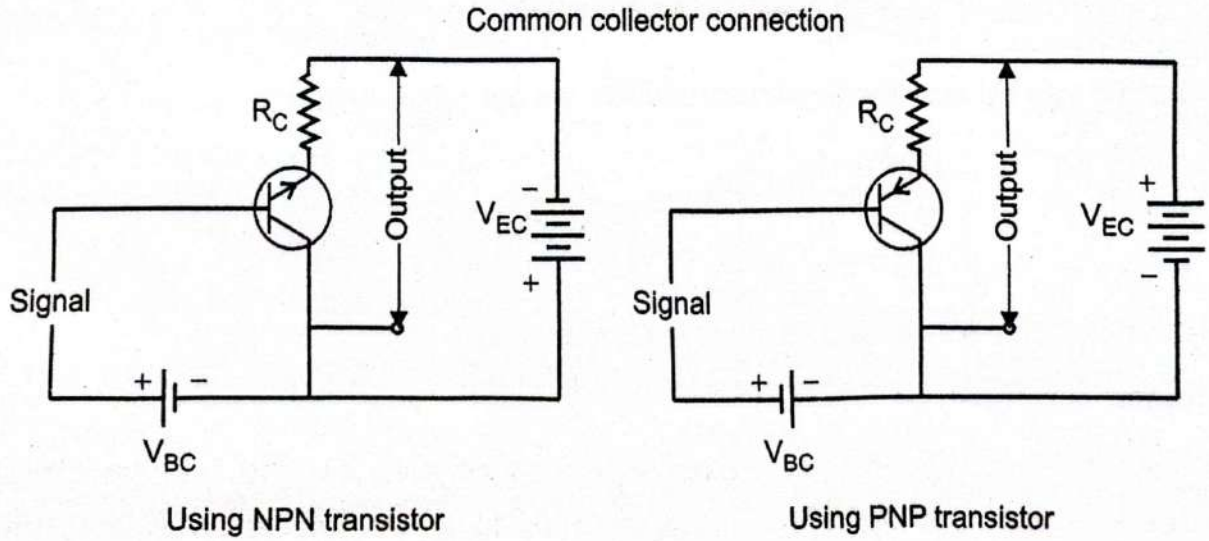


Fig. 4.16: NPN transistor and PNP transistor as CC amplifier

Current Amplification Factor (γ):

The ratio of change in emitter current (ΔI_E) to change in base current (ΔI_B) known as the Current Amplification factor in CC configuration. It is denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

The current gain in CC configuration is the same as in CE configuration.

The voltage gain in CC configuration is always less than 1.

Relation between γ and α:

Let us derive the relation between collector current amplification factor (γ) and emitter current amplification factor (α).

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

and $$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of ΔI_B, then collector current amplification factor (γ) is

$$\gamma = \frac{\Delta I_E}{(\Delta I_E - \Delta I_C)}$$

Dividing by (ΔI_E) to Numerator and Denominator, then

$$\gamma = \frac{\Delta I_E}{(\Delta I_E - \Delta I_C)}$$

$$\gamma = \frac{\left[\frac{\Delta I_E}{\Delta I_E}\right]}{\left[\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}\right]}$$

$$\gamma = \frac{1}{[1-\alpha]}$$

This equation represents the relation between γ and α.

Expression for Collector Current (I_C):

We know, $(I_C = \alpha I_E + I_{CBO})$ $I_E = I_B + I_C$

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \left[\frac{1}{(1-\alpha)}\right] I_B + \left[\frac{1}{(1-\alpha)}\right] I_{CBO}$$

$$I_E = [1 + \beta]\, I_B + [1 + \beta]\, I_{CBO}$$

I_C is approximately equal to I_E.

Then, $I_C = [1 + \beta]\, I_B + [1 + \beta]\, I_{CBO}$

This is the expression for collector current.

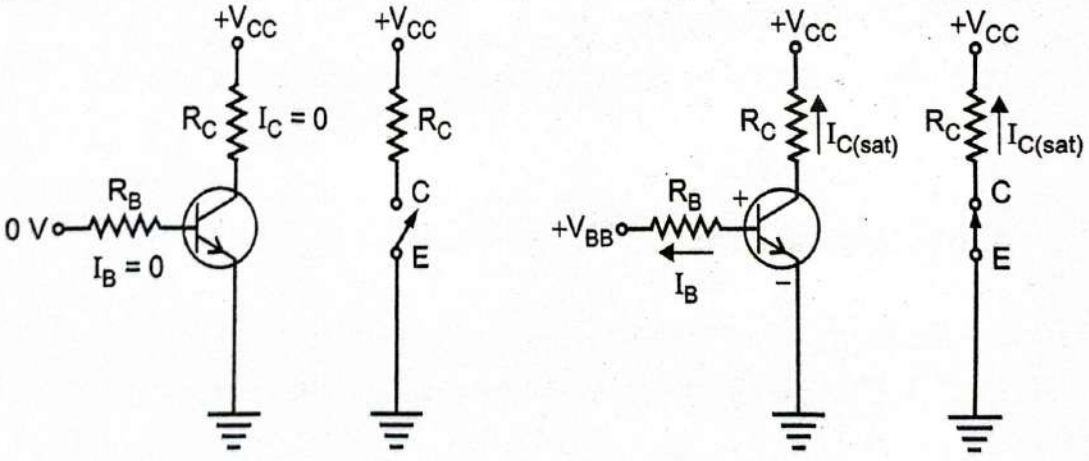
Characteristics of CC Configuration (Refer Fig. 4.13)

- This configuration provides current gain and no voltage gain.
- In CC configuration, the input resistance is high and the output resistance is low.
- The voltage gain provided by this circuit is less than 1.
- The sum of collector current and base current equals emitter current.
- The input and output signals are in phase.
- This configuration works as a non-inverting amplifier output.
- This circuit is mostly used for impedance matching. That means, to drive a low impedance load from a high impedance source.

4.6 SWITCHING OF BJT

4.6.1 BJT as a Switch

Below is a circuit arrangement to use the BJT as a switch.



(a) Cutoff-open switch **(b) Saturation-closed switch**

Fig. 4.17: BJT as a switch

The Collector terminal is biased with V_{CC} through R_C and the base terminal is biased with V_{BB} through R_B. R_B and R_C decides the transistor to work in saturation and cut-off region with respect to V_{BB}. The switching action of transistor is discussed as follows.

Case (i): Cut-off

If $V_{BB} = 0$, based current is zero and hence the collector current through the transistor is zero leading the collector to emitter voltage is equal to the applied voltage VCC, hence the terminals collector and emitter act as an open circuit called OFF switch.

i.e., $V_{CE(saturation)} = VCC$ ... (1)

Case (ii): Saturation

When a positive voltage of sufficient magnitude is applied across the base terminal, base to emitter junction conducts and sufficient base current will drive the transistor to the saturation region and maximum collector current flows through the device. Hence, the collector to emitter terminal acts as a short circuit and is called an ON switch.

i.e., $$I_{C(saturation)} = \left[\frac{V_{CC} - V_{CE(saturation)}}{R_C}\right] \quad \ldots (2)$$

$$V_{CE(saturation)} = 0$$

Then $$I_{C(saturation)} = \frac{V_{CC}}{R_C} \quad \ldots (3)$$

Example to Show Switch Action of Transistor:

Consider $V_{CC} = 5V$, $R_C = 1\ K\Omega$, $\beta = 100$, we know that, $V_{CE} = V_{CC} - I_C R_C$

If $I_B = 0$, $V_{CE} = V_{CC} \Rightarrow 5V$ (cut off)

If $I_B = 10\mu A$, $V_{CE} = 4V$, (Active region)

If $I_B = 20\mu A$, $V_{CE} = 3V$, (Active region)

If $I_B = 30\mu A$, $V_{CE} = 2V$, (Active region)

If $I_B = 40\mu A$, $V_{CE} = 1V$, (Active region)

If $I_B = 50\mu A$, $V_{CE} = 0V$, (Saturation)

i.e., $10\ \mu A < I_B < 50\ \mu A \Rightarrow$ Active region

$I_B > 50\mu A \Rightarrow$ switch

4.7 NUMERICALS

Problem 4.1: *A common base transistor amplifier has an input resistance of 20 Ω and an output resistance of 100 kΩ. The collector load is 1 kΩ. If a signal of 500 mV is applied between the emitter and base, find the voltage amplification. Assume α_{ac} is nearly one.*

Solution: Fig. 4.18 shows the conditions of the problem. In this, the output resistance is very high as compared to the input resistance, since the input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.

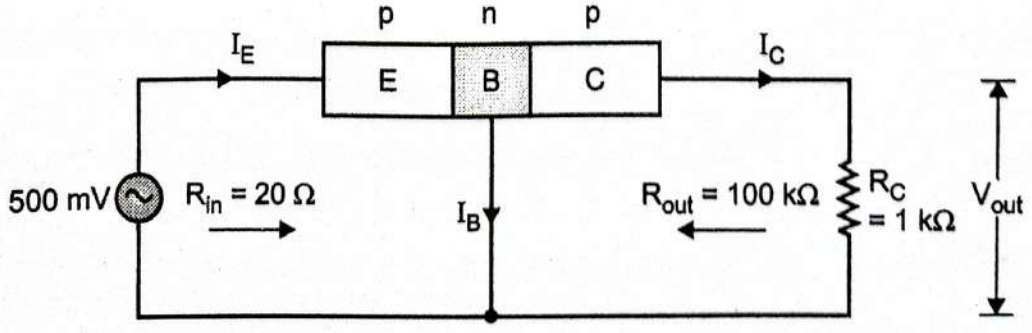


Fig. 4.18

Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500\text{ mV}}{20\ \Omega} = 25\text{ mA}$

Since, α_{ac} is nearly 1, output current, $I_C = I_E = 25$ mA

Output voltage,

$$V_{out} = I_C R_C = 25\text{ mA} \times 1\text{ k}\Omega = 25\text{ V}$$

$\therefore$ Voltage amplification,

$$A_V = \frac{V_{out}}{\text{signal}} = \frac{25\text{ V}}{500\text{ mV}} = \mathbf{50}$$

Problem 4.2: *In a common base connection, I_E = 1 mA, I_C = 0.95 mA. Calculate the value of I_B*

Solution: Using relation,

$$I_E = I_B + I_C$$

$$1 = I_B + 0.95$$

$$I_B = 1 - 0.95$$

$$= \mathbf{0.05\text{ mA}}$$

Problem 4.3: *Find the value of β if (i) $\alpha = 0.9$ (ii) $\alpha = 0.98$ (iii) $\alpha = 0.99$*

Solution: (i) $\alpha = 0.9$ $\beta = \frac{\alpha}{(1-\alpha)} = \frac{0.9}{(1-0.9)} = \mathbf{9}$

(ii) $\alpha = 0.98$ $\beta = \frac{\alpha}{(1-\alpha)} = \frac{0.98}{(1-0.98)} = \mathbf{49}$

(iii) $\alpha = 0.99$ $\beta = \frac{\alpha}{(1-\alpha)} = \frac{0.99}{(1-0.99)} = \mathbf{99}$

Problem 4.4: *Calculate I_E in a transistor for which $\beta = 50$ and $I_B = 20\ \mu A$*

Solution: $\beta = \frac{I_C}{I_B}$ then $I_C = \beta I_B$

$$I_C = 50(20 \times 10^{-6}) = (1000)10^{-6} = 10^{-3} = 1\text{ mA}$$

$$\alpha = \frac{I_C}{I_E} \text{ (We know, } \alpha = 0.98)$$

Using relation $I_E = \frac{I_C}{\alpha} = \frac{(1 \times 10^{-3})}{0.98} = 1.02 \times 10^{-3} = 1.02\text{ mA}$

Or, Using relation,

$$I_E = I_B + I_C$$

$$= 0.020\text{ mA} + 1\text{ mA} = \mathbf{1.02\text{ mA}}$$

Problem 4.5: *Find α rating of transistor shown in below Fig. 4.19. Determine value of I_C using both α and β rating of the transistor.*

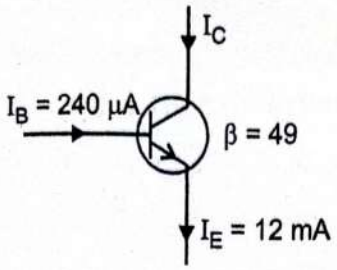


Fig. 4.19

Solution:
$$\alpha = \frac{\beta}{(\beta + 1)} = \frac{49}{(49 + 1)} = 0.98$$

The value of collector current can be found using either α or β rating as under,

$$I_C = \alpha I_E = (0.98)\ 12\ mA = 11.76\ mA$$

$$I_C = \beta I_B = (49)\ 240\ \mu A = \mathbf{11.76\ mA}$$

Problem 4.6: *In a transistor, $I_B = 68\ \mu A$, $I_E = 30$ mA and $\beta = 440$. Determine rating (α) of the transistor. Then determine value of I_C using both α rating and β rating of transistor.*

Solution:
$$\alpha = \frac{\beta}{(\beta + 1)} = \frac{440}{(440 + 1)} = 0.9977$$

$$I_C = \alpha I_E = (0.9977)\ 30\ mA = 29.93\ mA$$

$$I_C = \beta I_B = (440)\ 68\ \mu A = \mathbf{29.92\ mA}$$

QUESTIONS

1. What is a transistor? Give its circuit symbol.
2. A transistor operating in the active region, although the collector junction is reverse biased the collector current is quite large. Explain.
3. Define current gain.
4. If the base current in the transistor is 30 micro amps when the emitter current is 2 mA. What value of α and β?
5. Give the relation between α and β.
6. Define α and β. Give the relationship between them.
7. List some applications of BJT.
8. Justify the cutoff and active region of a transistor.
9. Draw the Input characteristics of a transistor and resistance in CE configuration.
10. Draw the Input characteristics of a transistor and resistance in CB configuration.
11. Draw the Input characteristics of a transistor and resistance in CC configuration.

12. Among CE, CB and CC configurations, which is the most popular? Justify?
13. What is biasing of a transistor? Why it is needed?
14. In a common base, emitter current is 1 mA, I_{CBO} = 50 μA, α = 0.92 Find collector current.
15. Describe how switching achieved using a BJT, Justify it?
16. What are the bias conditions to operate a transistor in active mode?
17. Draw input characteristics of a transistor in CB configuration.
18. Draw output characteristics of a transistor in CE configuration.
19. Describe two applications of BJT.
20. Explain the operation of NPN and PNP transistors.
21. Distinguish between the different types of transistor configurations.
22. Draw transistor mode circuit diagrams in CB, CE and CC Modes.
23. Can a transistor be used as a switch?
24. Draw the symbols for NPN and PNP transistor.
25. Draw IV characteristics of BJT.
26. A transistor has α = 0.99. Calculate the base circuit, if the emitter current is 8mA.
27. Find α for each β = 190 and β = 50.
28. Find α for each β = 100 and β = 27.
29. Explain the working of an NPN transistor with a neat circuit diagram.
30. Draw and Explain I-V characteristics of BJT.

Module - V

FIELD EFFECT TRANSISTORS

Syllabus:

- *Field-Effect Transistors (FETs) - FET types: JFET, MOSFET, Structure and operation MOSFETs in Detail-MOSFET structure, Enhancement and depletion modes, Threshold voltage, MOSFET Applications - MOSFET as a switch.*

Objectives:

- *To build foundation of Field effect transistors and their applications.*

Outcome:

- *Learner will be able to Plot I-V characteristics and understand applications of FETs.*

List of Contents:

5.1 *Introduction to FET*

5.2 *Types of Field Effect Transistors*

5.3 *Structure and Operation of JFET*

5.4 *Application of JFET*

5.5 *Introduction to MOSFET*

5.6 *Structure and Operation of MOSFET*

5.7 *Modes of MOSFET*

5.8 *MOSFET Applications and Threshold Voltage*

5.8.1 *MOSFET as a Switch*

5.9 *Numericals*

- *Questions*

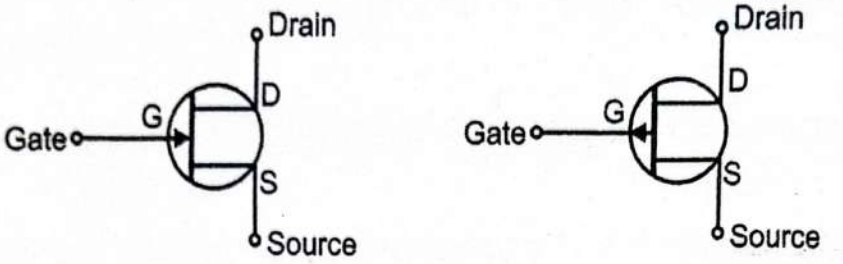
5.1 INTRODUCTION TO FET

We are surrounded by numerous electronic devices all around and now everything is just a click away from us. We went from desktop computers to supercomputers as technology advanced and during this long journey, a transistor, an electronic component, played a significant role in this evolution. Field Effect Transistor (FET) is a crucial electronic component. As of now, FET transistors are widely used transistors, providing the main active component in many integrated circuits. It is a voltage controlled device. It has several advantages: less power consumptions and high input impedance, which is used in many devices to operate.

Field-Effect Transistor is a three terminal unipolar device that consists of a channel made of either p-type or n-type material as the main substrate, with two electrodes connected at either end, namely the drain or source. Hence the current conduction in a FET is done by either electrons or holes.

FET Terminals:

Though FET is a three terminal device that has a Source, the Gate and Drain. The **Source** terminal in FET is analogous to the Emitter in BJT, while the **Gate** is analogous to the Base and the **Drain** to the Collector. The symbols of a FET for both N and P channel types are as shown below.



Symbol of n-channel FET Symbol of p-channel FET

Fig. 5.1: FET symbols

Source (S)

- The Source terminal is one through which the carriers enter the channel.
- This is analogous to the emitter terminal in a Bipolar Junction Transistor.
- The Source terminal designated as S.
- The current entering the channel at the Source terminal is indicated as I_S.

Gate (G)

- The Gate terminal plays a key role in the function of FET by controlling the current through channel.
- By applying an external voltage at Gate terminal, the current through it can be controlled.
- Gate is a combination of two terminals connected internally that are heavily doped.
- The channel conductivity is said to be modulated by the Gate terminal.
- This is analogous to the base terminal in a Bipolar Junction Transistor.
- The Gate terminal designated as G.
- The current entering the channel at Gate terminal is indicated as I_G.

Drain (D)

- The Drain terminal is one through which the carriers leave the channel.
- This is analogous to the collector terminal in a Bipolar Junction Transistor.
- The Drain to Source voltage is designated as V_{DS}.
- The Drain terminal can be designated as D.
- The current leaving the channel at the Drain terminal

5.2 TYPES OF FIELD EFFECT TRANSISTORS

FET and bipolar transistors are basically the same in appearance. A Field Effect Transistor (FET) operation depends on a controlled input voltage. Two types of FETs are available.

(i) Junction Field Effect Transistor (JFET)

(ii) Metal Oxide Semiconductor FET (MOSFET)

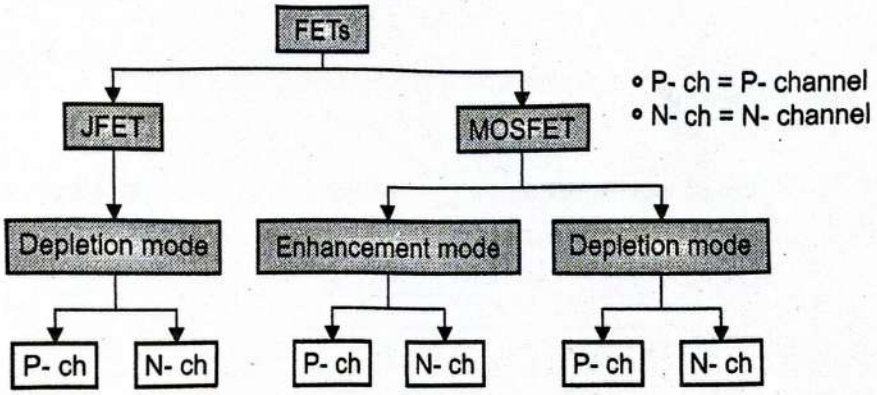


Fig. 5.2: Types of FET

JFET operate based on the movement of electrons or holes, which are the majority carriers. These transistors are constructed using a silicon bar that contains PN junctions on its sides. JFET is just like a normal FET.

To better understand the JFETs, some essential points to keep in mind.

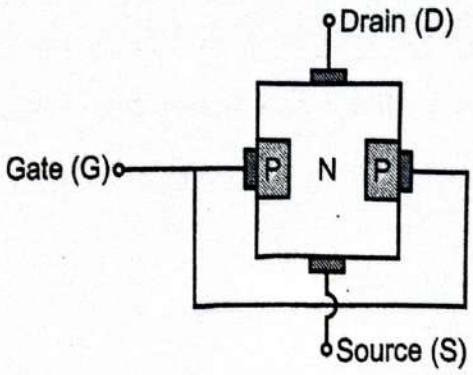
Gate is heavily doped. The majority of carriers enter the semiconductor bar through the source, which serves as the entry point. On the other hand, the drain acts as an exit point, allowing the majority of carriers to leave the semiconductor bar. The channel refers to the N-type material area that facilitates the flow of majority carriers from the source to the drain.

5.3 STRUCTURE AND OPERATION OF JFET

In the realm of semiconductor devices, there are two commonly used types of JFETs: N-channel JFET and P-channel JFET. A p-type material is added to the n-type substrate in an n-channel FET, whereas an n-type material is added to the p type substrate in an p-channel FET. Both variants play a crucial role in various electronic applications. Hence it is enough to discuss one type of FET to understand both.

N-Channel FET

The N-channel FET is the most used Field Effect Transistor. For the fabrication of N-channel FET, a narrow bar of N-type semiconductor is taken on which P-type material is formed by diffusion on the opposite sides. These two sides are joined to draw a single connection for the gate terminal. These two gate depositions of p-type materials form two PN diodes. The area between gates is called as a **channel**. The majority carriers pass through this channel. Hence the cross sectional view of FET is understood as in the following Fig. 5.3.



Structure of N-channel FET

Fig. 5.3: N chanel FET

Ohmic contacts are made at the two ends of the n-type semiconductor bar, which form the source and the drain. The source and the drain terminals may be interchanged.

Biasing of JFET

There are two methods in use for biasing the JFET:

(i) Self-Bias Method

(ii) Potential Divider Method or Voltage Divider Method

(i) Self-Bias Method: The following Fig. 5.4 shows the self-bias method for n-channel JFET. The drain current flows through R_S and produces the required bias voltage. Therefore, R_S acts as the bias resistor.

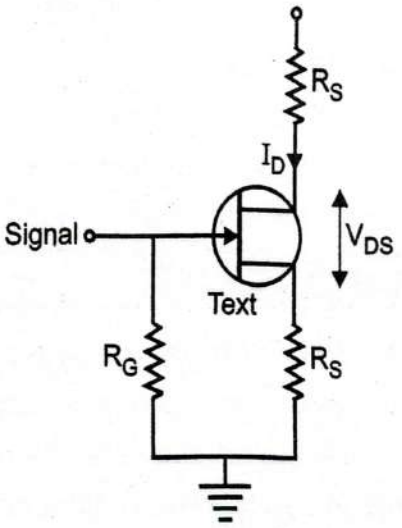


Fig. 5.4: Self-Bias method of FET

Hence, voltage across the bias resistor,

$$V_S = I_D R_S$$

As we know, gate current is negligible, the gate terminal is at DC ground, $V_G = 0$.

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S$$

V_{GS} keeps the gate negative with respect to the source.

(ii) Voltage Divider Method:

The following Fig. 5.5 shows the voltage-divider method for biasing the JFETs. Here, resistors R_1 and R_2 form a voltage-divider circuit across drain supply voltage (V_{DD}) and it is more or less identical to the one used in transistor biasing.

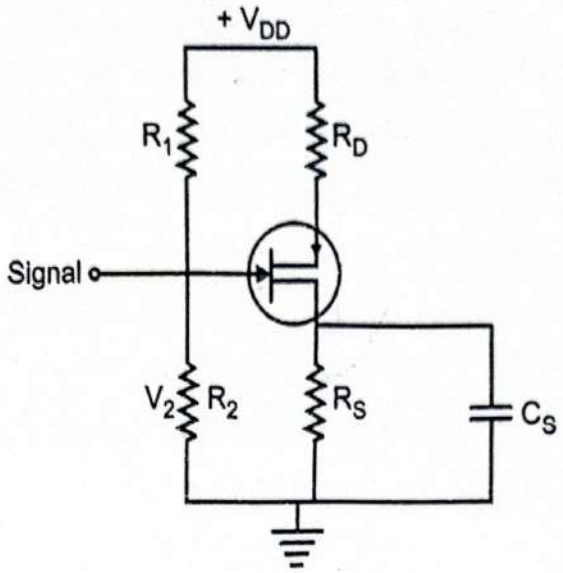


Fig. 5.5: Voltage divider method of FET

The voltage across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}(R_1 + R_2)}{R_2}$$

$$= V_2 + V_{GS} + I_D + R_S$$

or

$$V_{GS} = V_2 - I_D R_S$$

The circuit is designed so that V_{GS} is always negative. Following equation used to determine the operating point:

$$I_D = \frac{(V_2 - V_{GS})}{R_S}$$

and

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

Working of JFET:

Before going into the operation of JFET one should understand how the depletion layers are formed. For this, the voltage at the gate terminal, say V_{GG} is reverse biased while the voltage at drain terminal, say V_{DD} is not applied.

In Case 1: When V_{GG} is reverse biased and V_{DD} is not applied, the depletion regions between P and N layers tend to expand. This happens as the negative voltage applied, attracts the holes from the p-type layer towards the gate terminal.

In Case 2: When V_{DD} is applied at a positive terminal to drain and negative terminal to the source and V_{GG} is not applied, the electrons flow from source to the drain which constitute the drain current I_D.

Let us to understand what happens when both the supplies are given.

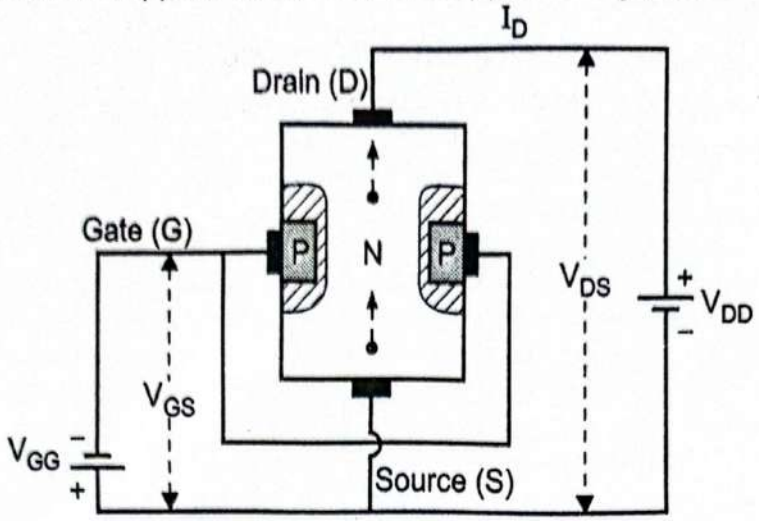


Fig. 5.6: FET operation

The supply at the gate terminal makes the depletion layer grow and the voltage at the drain terminal allows the drain current from the source to drain terminal.

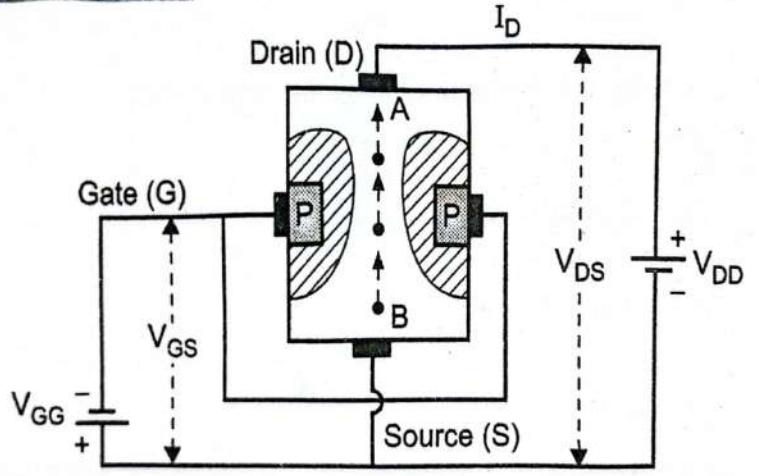


Fig. 5.7: FET operation with increase voltage

Suppose the point at the source terminal is B and the point at the drain terminal is A; then the resistance of the channel will be such that the voltage drop at the terminal A is greater than the voltage drops at the terminal B. Which means,

$$V_A > V_B$$

Hence the voltage drop is being progressive through the length of the channel. So, the reverse biasing effect is stronger at the drain terminal than at the source terminal. This is why the depletion layer tends to penetrate more into the channel at point A than at point B, when both V_{GG} and V_{DD} are applied.

Operation of JFET: Depletion Mode

As the width of the depletion layer plays an important role in the operation of FET, the name depletion mode of operation implies. We have another mode called enhancement mode of operation, which will be discussed in the operation of MOSFETs. But **JFETs have only a depletion mode** of operation.

Let us consider that there is no potential applied between gate and source terminals and a potential V_{DD} is applied between drain and source. Now, a current I_D flows from drain to source terminal, at its maximum as, channel width is more. Let the voltage applied between the gate and source terminal, V_{GG} be reverse biased. This increases the depletion width, as discussed above. As the layers grow, the cross-section of the channel decreases and hence the drain current I_D also decreases.

When this drain current is further increased, a stage occurs where both the depletion layers touch each other and prevent the current I_D flow. This is clearly shown in the following Fig. 5.8.

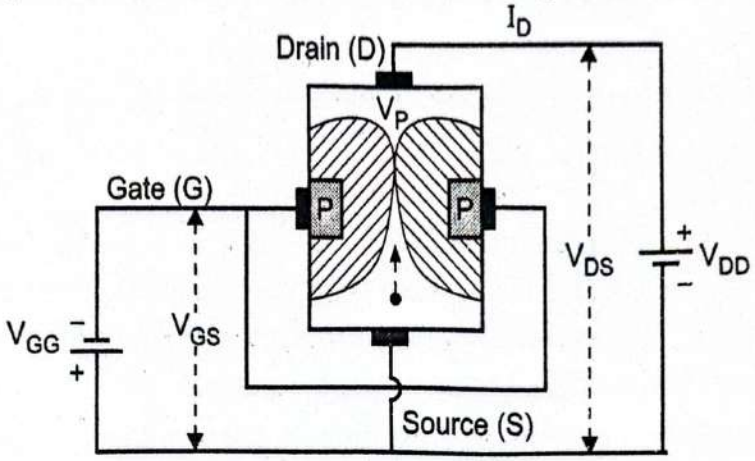


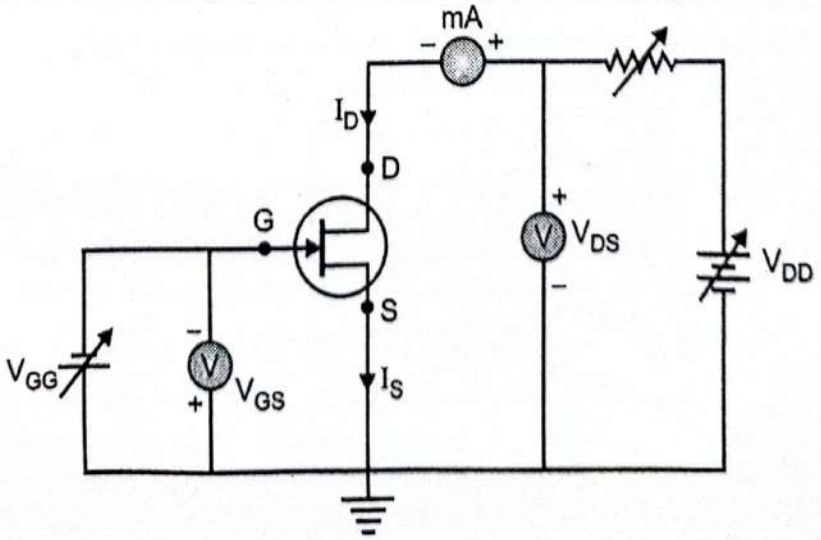
Fig. 5.8: Channel blocked in FET operation

The voltage at which both these depletion layers literally "touch" is called the "**Pinch off voltage**". It is indicated as V_P. The drain current is literally nil at this point. Hence the drain current is a function of reverse bias voltage at gate. Since gate voltage controls the drain current, FET is called a **voltage controlled device**. This is more clearly understood from the drain characteristics curve.

Characteristics of JFET

1. Drain (Output) Characteristics:

Output characteristics of JFET are drawn between drain current (I_D) and drain source voltage (V_{DS}) at constant gate source voltage (V_{GS}), shown in the following Fig. 5.9.



5.9 (a): Block diagram of FET operation

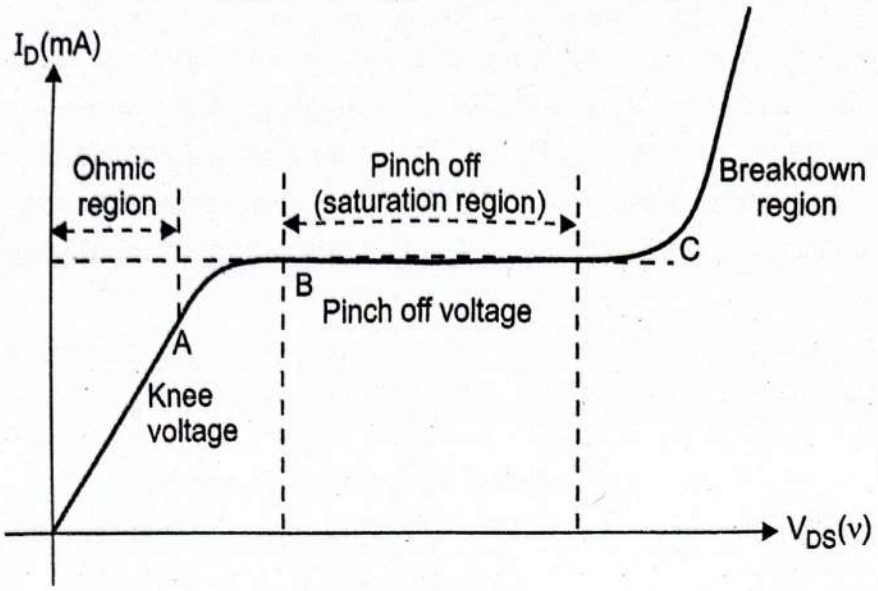


Fig. 5.9 (b): Drain curve

When the voltage between gate and source is zero (V_{GS} = 0) or they are shorted, then the current I_D from source to drain is also nil, as there is no V_{DS} applied. As the voltage between drain and source V_{DS} is increased, the current flow I_D from source to drain increases. This increase in current is linear up to a certain point A, known as Knee Voltage.

The gate terminals will be under reverse biased condition and as I_D increases, the depletion regions tend to constrict. This constriction is unequal in length, making these regions come closer at drain and farther at drain, which leads to pinch off voltage. The pinch off voltage is defined as the minimum drain to source voltage where the drain current approaches a constant value saturation value. The point at which this pinch off voltage occurs is called the Pinch off point, denoted as B.

As V_{DS} is further increased, the channel resistance also increases in such a way that I_D practically remains constant. The region BC is known as the saturation region or amplifier region. All these, along with the points A, B and C are plotted in the graph above.

The drain characteristics are plotted for drain current I_D against drain source voltage V_{DS} for different values of V_{GS}. The overall drain characteristics for such various input voltages are as given under. As the negative gate voltage controls the drain current, FET is called as a Voltage controlled device. The drain characteristics indicate the performance of a FET.

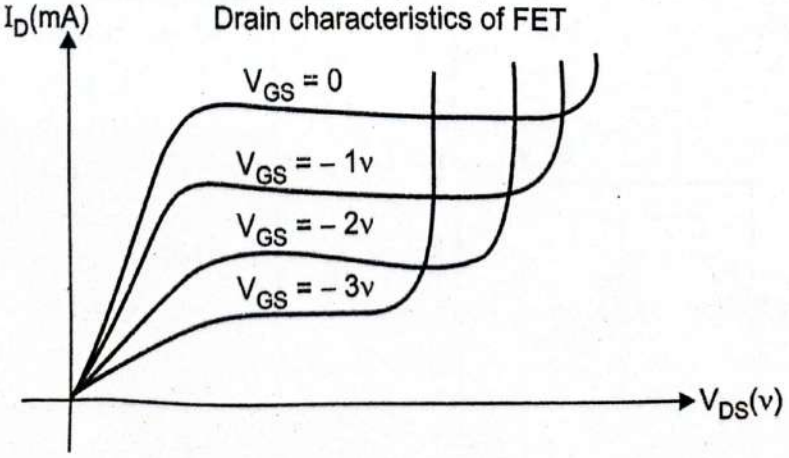


Fig. 5.10: Drain curve at various V_{GS}

Operating Region of FET

- **Ohmic Region:** This prevents the channel from being pinched off and causes the current I_D to rise because the V_{DS} value is greater than zero and lower than V_P. At the point when we increase the gate source voltage (V_{GS}), the channel conductance falls and the resistance is increased. In this way, the depletion regions will spread more, creating a narrow channel. The channel resistance changes by and large from 100 ohms to 10 K-ohms and controls the voltage. Thus, transistors act as voltage-controlled resistors in this region.
- **Saturation Region ($V_{DS} > V_{GS} - V_P$):** This region starts from where V_{DS} is greater than V_{GS} minus V_P; here V_P is the pinch-off voltage. Around here, the drain current I_D completely depends on the V_{GS} and is not an element of the V_{DS}. The FET operates in this region to amplify the signal with respect to switching operations as well. From Fig. 5.10, it is seen that when V_{GS} is zero, the maximum current I_D flows. The drain current decreases when the V_{GS} is made more negative. At a specific value of V_{GS}, the drain current flows constantly through the device. Consequently, this region is also called the constant current region.
- **Cutoff Region ($V_{GS} < V_P$):** The region in which the drain current I_D is zero and the device is off is known as the cutoff region ($V_{GS} < V_P$). The gate source voltage V_{GS} is less than the pinch-off voltage V_P. This implies the value of V_{GS} is more negative than V_P. As a result, the channel closes, preventing the device from receiving any current.
- **Breakdown Region:** This is the last and terminal region of the characteristics curve for the field effect transistor, you can see this region in the right corner. At this point, the voltage shown by the V_{DS} between the drain and source is very high. The voltage is sufficiently high that the conductive channel is broken and maximum current goes through the channel into the drain.

2. Transfer Characteristics of JFET:

The transfer characteristics of a JFET plotted between the drain current (I_d) and drain source voltage (V_{ds}). It can be determined by keeping V_{ds} constant and drain current can be observed by changing the gate source voltage. So we can observe that when V_{gs} is increased, the drain current I_d decreases. When the drain source voltage is constant, it can be observed that the value of the drain current varies inversely with respect to the gate source voltage. The above transfer characteristics curve of JFET is described below, it can be observed that the value of drain current varies inversely with respect to gate-source voltage when the drain-source voltage is constant.

The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear as shown in the below Fig. 5.11. This relationship is defined by Shockey's equation.

Transfer Characteristics for n-Channel JFET:

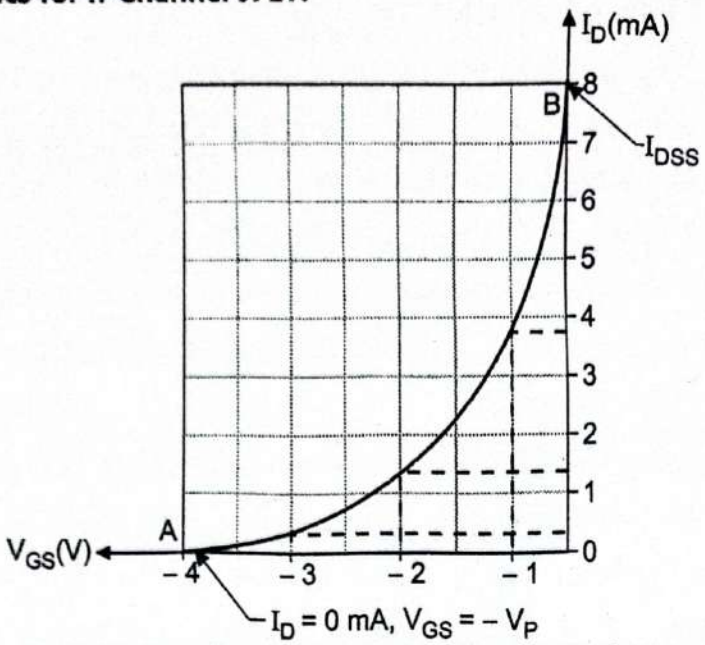


Fig. 5.11: Transfer characteristics for n-channel JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term of the equation will result in a non-linear relationship between I_D and V_{GS} producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From the equation we can also write,

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

In the equation values of I_{DSS} and V_P are constants, value of V_{GS} controls I_D.

A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS(off)}$ and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at V_{GS} = 0). Thus, this curve shows the operating limits of a JFET. These are:

I_D = 0 when $V_{GS} = V_{GS(off)}$

$I_D = I_{DSS}$ when V_{GS} = 0

Transfer Characteristics of p-Channel JFET:

The below Fig. 5.12 shows the transfer characteristics of p-channel JFET. It is identical to the transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

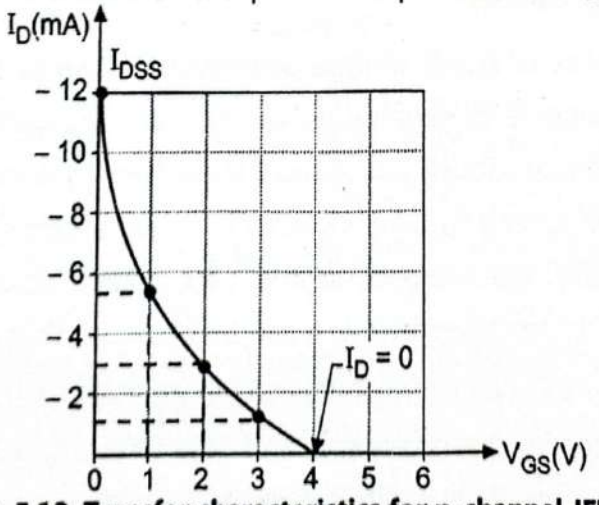


Fig. 5.12: Transfer characteristics for p-channel JFET

Parameters of JFET:

- AC drain resistance (Rd)
- Transconductance (gf)
- Amplification factor (μ)

The drain characteristics plotted above are used to obtain the values of drain resistance, transfer characteristics are used to obtain the values of transconductance. From drain resistance (Rd) and transconductance values we can calculate amplification factor.

AC Drain Resistance (Rd): It's a ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage (V_{GS}).

Mathematically it is expressed as,

$$Rd = \frac{(\Delta V_{DS})}{(\Delta I_D)} \text{ at constant } V_{GS}$$

Transconductance (gf): It's a ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage (V_{DS}).

Mathematically it is expressed as,

$$gf = \frac{(\Delta I_D)}{(\Delta V_{GS})} \text{ at constant } V_{DS}$$

Amplification Factor (μ): It's a proportion of progress in channel drain-source voltage (ΔV_{DS}) to change in gate-source voltage (ΔV_{GS}) at constant drain current (I_D).

Mathematically it is expressed as,

$$\mu = \frac{(\Delta V_{DS})}{(\Delta V_{GS})} \text{ at constant } I_D$$

It a product of drain resistance (Rd) and Transconductance (gf)

$$\mu = Rd \times gf$$

FET as a Switching Circuits:

From the above discussion, the FET can be used as a switch by operating it in two regions: the cutoff region and the saturation region.

- At the point when the V_{GS} is zero, the FET works in the saturation region and maximum current flows through it. Consequently, it is like a fully turned-on condition.
- Similarly, when the V_{GS} applied is more negative than the pinch-off voltage, the FET works in the cutoff region and does not allow any current to flow through the device.
- Consequently FET is in completely OFF condition. FET can be used as a switch in different configurations.
- FET as a Shunt Switch.
- FET as a Series Switch.

FET as a Shunt Switch:

At the point when the V_{GS} applied is zero, the FET is turned on by operating in the saturation region and its resistance is very small, 100 ohms. Output voltage across the FET is,

$$V_{OUT} = V_{in}\left[\frac{R_{DS}}{(R_D + R_{DS(ON)})}\right]$$

The output voltage is considered zero due to the large resistance R_D.

At the point when we apply the negative voltage, which is equivalent to the pinch-off voltage at the gate, the FET operates in the cutoff region and acts as a high-resistance device and the output voltage is equivalent to the input voltage.

FET as a Series Switch:

A FET acts as a series switch in this circuit. It acts as a closed switch if the control voltage is zero and an open switch if the control voltage is negative. At the point when the FET is ON, the input signal will show up at the output and when it is OFF, the output is zero.

5.4 APPLICATION OF JFET

Junction Field Effect Transistor (JFET) has several applications, including

- Constant current source
- Buffer amplifier
- Electronic switch
- Phase shift oscillator
- High impedance wide band amplifier
- Mixer circuits of TV and FM receivers due to low intermodulation distortions
- Voltage-variable resistors in OP-AMPS, tone control circuits and JFET voltmeter design
- Timer circuits, as they offer high isolation between their gate and drain terminals

Features of JFET

The following are the varied features of a Field Effect Transistor.

- **Unipolar:** It is unipolar, as either holes or electrons are responsible for conduction.
- **High Input Impedance:** input current in a FET flows due to reverse bias. Hence it has high input impedance.
- **Voltage Controlled Device:** As the output voltage of a FET is controlled by the gate input voltage, FET is called the voltage controlled device.
- **Noise:** It is low. There are no junctions present in conduction path. Hence, noise is lower as compared to BJTs.
- **Gain:** It is characterized as transconductance (Transconductance is the ratio of change in output current to change in input voltage).
- **Output Impedance:** It is low.

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- **Output Impedance:** It is low.

Comparison between FET and BJT

To prefer a FET over a BJT, there should be few advantages to using FETs, rather than BJTs. The advantages of FET over BJT are summarized in Table 5.1.

Table 5.1

FET	BJT
It is a unipolar device.	It is a bipolar device.
It's a three terminals as source, gate and drain.	It's a three terminals as emitter, base and collector.
It is voltage driven device.	It is current driven device.
It has lower voltage drop.	It has a higher voltage drop.
It has lower gain bandwidth product.	It has higher gain bandwidth product.
It has high input impedance.	It has low input impedance.
Low noise level.	High noise level.
Better thermal stability.	Less thermal stability.
Gain characterized by transconductance.	Gain characterized by voltage gain.
FET has a smaller size.	BJT has a bigger size.

5.5 INTRODUCTION TO MOSFET

MOSFET (metal-oxide-semiconductor field-effect transistor) was fabricated for the first time in 1960, only a year after the beginning of the integrated circuit era in 1959. The MOSFET became the basic building block of Very Large-Scale Integrated (VLSI) circuits, therefore becoming the most important microelectronic device. Huge investments have been made in what is known as CMOS technology, a technology used to manufacture circuits consisting of complementary pairs of MOSFETs. Those investments, having been quite favorable, consequently led to the rapid progress in computers, supercomputers, smartphones and communication integrated circuits that we have seen from decade to decade.

However, the application of MOSFETs is not limited to VLSI circuits. MOSFETs play an important role in power-electronic circuits and are becoming increasingly popular and suitable for microwave applications.

FETs have a few disadvantages, like high drain resistance, moderate input impedance and slower operation. To overcome these disadvantages, the MOSFET, which is an advanced FET, is invented. MOSFET stands for Metal Oxide Silicon Field Effect Transistor or Metal Oxide Semiconductor Field Effect Transistor. This is also called an IGFET meaning Insulated Gate Field Effect Transistor. This is operated in both depletion and enhancement modes of operation.

5.6 STRUCTURE AND OPERATION OF MOSFET

The construction of a MOSFET is a bit similar to that of a FET. An oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as an insulator (SiO_2 insulates from the substrate).

Hence, the MOSFET has another name IGFET. In the construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region. Depending upon the substrate used, they are called **P-type** and **N-type** MOSFETs. The following Fig. 5.13 shows the construction of a MOSFET.

MOSFET Construction:

MOSFET is a transistor that is used as a switch or amplifier and in many other applications. The basic construction of a MOSFET can be explained as below:

- **Substrate:** MOSFET is constructed on a silicon wafer that is it acts as a base of the device.
- **SiO_2:** A thin layer of insulating material is formed with SiO_2 for the exchange of electrons and holes.
- **Gate Terminal:** A gate terminal is formed on the insulating layer. This controls the flow of current between the drain and source with the help of gate voltage.
- **Source and Drain Terminals:** These are created on either side of the gate. These are basically doped regions.
- **Channel:** The region between the gate, drain and source is known as the channel which controls the flow of charge among them.

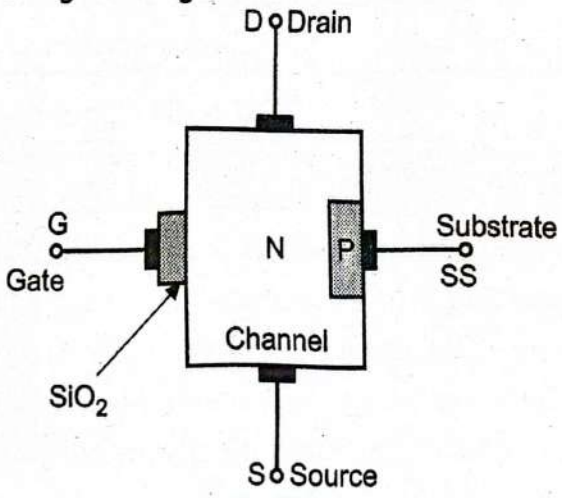


Fig. 5.13: MOSFET structure

The voltage at the gate that controls the operation of the MOSFET. In this case, both positive and negative voltages can be applied to the gate as it is insulated from the channel. With negative gate bias voltage, it acts as the **Depletion MOSFET** while with positive gate bias voltage it acts as an **Enhancement MOSFET**.

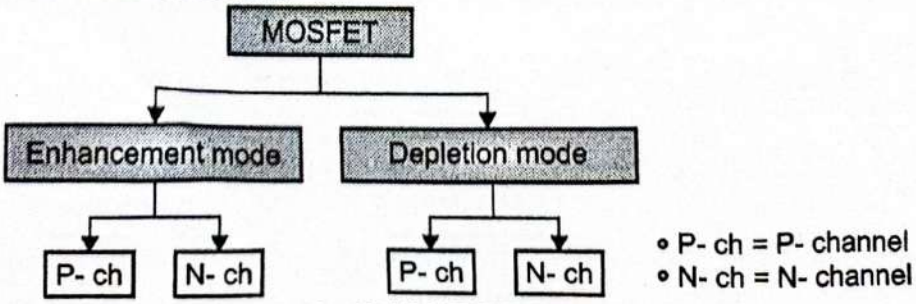
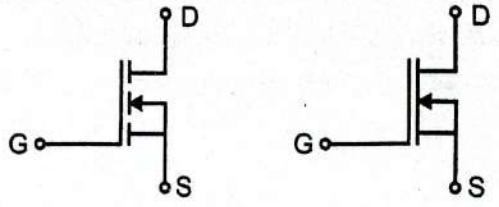


Fig. 5.14: MOSFET types

N-channel MOSFETs are called **NMOS**. The symbols for N-channel MOSFET are as below.

Symbols of N-channel MOSFET

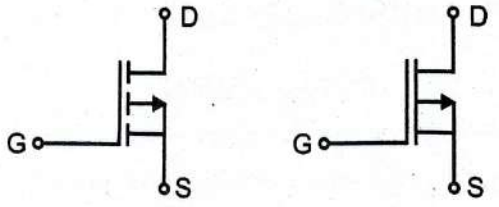


Enhancement mode Depletion mode

Fig. 5.15: N channel MOSFET types

P-channel MOSFETs are called **PMOS**. The symbols for P-channel MOSFET are as below.

Symbols of P-channel MOSFET



Enhancement mode Depletion mode

Fig. 5.16: P channel MOSFET types

When we provide external voltage in the channel, it can either increase or decrease the amount of charge carriers in the channel. If the number of charge carriers increases, it is known as enhancement type MOSFET. But if the number of charge carriers decreases, then it is known as depletion type MOSFET.

Now these enhancement type and depletion type MOSFETs are further classified into p-channel and n-channel MOSFETs.

Enhancement Type MOSFET:

- In this type of MOSFET, no channel is present from the beginning and hence no current flows.
- But when the +ve voltage is more than the threshold voltage, it leads to an enhancement of a channel between the drain and source due to the gate voltage and thus it results in the conductivity of device.
- They are mostly used in digital applications.

Depletion Type MOSFET:

- In this type of MOSFET, a channel is present from the beginning, which means conduction of current is there.
- -ve voltage is applied to reduce the flow of current and this reduces the width of the channel.
- Not used commonly in devices.

Construction of N-Channel MOSFET

Let us consider an N-channel MOSFET to understand it's working. A lightly doped P-type substrate is taken into which two heavily doped N-type regions are diffused, which act as source and drain. Between these two N+ regions, there occurs diffusion to form an N-channel, connecting drain and source.

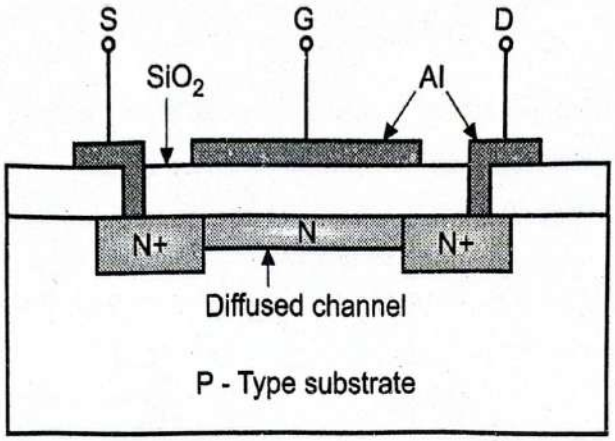


Fig. 5.17: Structure of N-channel MOSFET

A thin layer of Silicon dioxide (SiO_2) is grown over the entire surface and holes are made to draw Ohmic contacts for drain and source terminals. A conducting layer of aluminum is laid over the entire channel, upon this SiO_2 layer from source to drain, which constitutes the gate. The SiO_2 substrate is connected to the common or ground terminals. Because of its construction, the MOSFET has a much smaller chip area than the BJT, which is 5% of the occupancy when compared to the bipolar junction transistor. This device can be operated in modes. They are depletion and enhancement modes.

Construction of P-Channel MOSFET:

The construction and working of a PMOS is the same as an NMOS. A lightly doped n-substrate is taken into which two heavily doped P+ regions are diffused. These two P+ regions act as source and drain. A thin layer of SiO_2 is grown over the surface. Holes are cut through this layer to make contacts with P+ regions, as shown in the following Fig. 5.18.

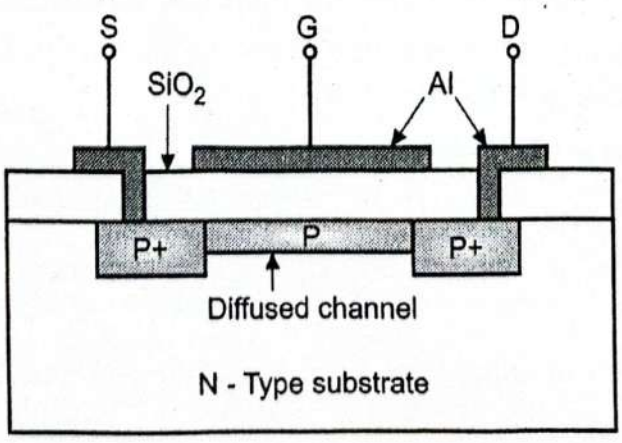


Fig. 5.18: Structure of P-channel MOSFET

Operation of MOSFET:

MOSFET is a type of transistor in which conductivity depends upon the semiconductor channel across the drain and source terminal. This semiconductor channel may be p-channel or n-channel depending upon the configuration of the MOSFET. It consists of three terminals: drain, source and gate. By applying some voltage across the gate and source, there forms an inversion layer or a channel between the drain and source if the voltage applied is threshold voltage. (Threshold voltage is the minimum required voltage for the conduction of current). If the applied voltage is less than the threshold voltage, no channel is formed. Hence current cannot flow in the MOSFET. This situation is called the Cutoff region (OFF) and after a certain level of voltage, the current becomes constant in the MOSFET. This condition is called a saturation point.

MOSFET is a voltage controlled device, so the thickness of the channel and the amount of current depend upon the voltage applied across the gate and source. If more voltage is applied, the width of the channel increases and more amount of current is able to flow through the device.

Characteristics of MOSFET

MOSFETs have two major characteristics:

1. Drain characteristics
2. Transfer characteristics

Working of N – Channel MOSFET (Depletion Mode):

For now, we have an idea that there is no PN junction present between the gate and channel in this, unlike a FET. We also observe that, in the diffused channel N between two N+ regions, the insulating dielectric SiO_2 and aluminum metal layer of the gate together form a parallel plate capacitor.

If the NMOS has to be worked in depletion mode, the gate terminal should be at negative potential while the drain is at positive potential, as shown in the following Fig. 5.19.

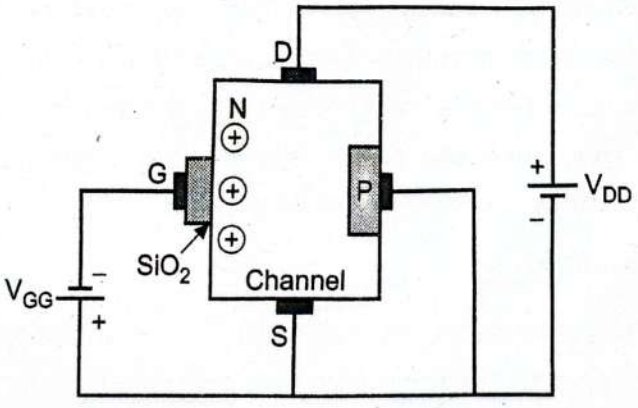


Fig. 5.19: Working of N-channel MOSFET in depletion mode

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some negative voltage applied at V_{GG}. Then the minority carriers i.e. holes, get attracted and settle near the SiO_2 layer. But the majority carriers, i.e., electrons, get repelled. With some amount of negative potential at V_{GG} a certain amount of drain current I_D flows through source to drain. When this negative potential is further increased, the electrons get depleted and the current I_D decreases. Hence the more negative the applied V_{GG}, the lesser the

value of drain current I_D will be. The channel nearer to the drain gets more depleted than at the source like in FET and the current flow decreases due to this effect. Hence it is called depletion mode MOSFET.

Working of N-Channel MOSFET (Enhancement Mode):

The same MOSFET can be worked in enhancement mode, if we can change the polarities of the voltage V_{GG}. So, let us consider the MOSFET with gate source voltage V_{GG} being positive as shown in the following Fig. 5.20.

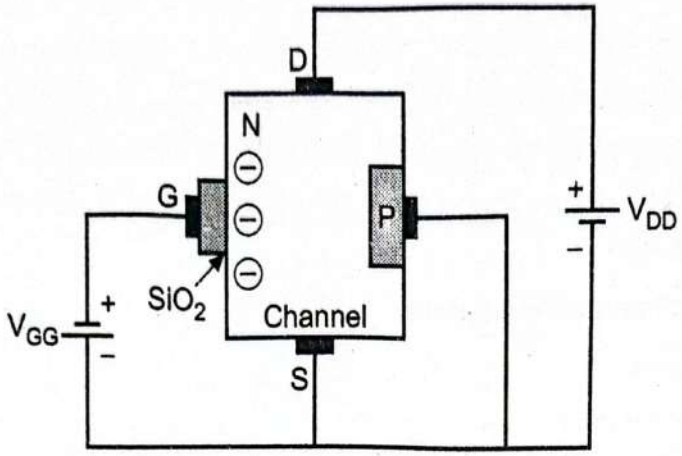


Fig. 5.20: Working of N-channel MOSFET in enhanced mode

When no voltage is applied between gate and source, some current flows due to the voltage between drain and source. Let some positive voltage be applied at V_{GG}. Then the minority carriers, i.e., holes, get repelled and the majority carriers i.e., electrons get attracted towards the SiO_2 layer.

With some amount of positive potential at V_{GG} a certain amount of drain current, I_D flows through source to drain. When this positive potential is further increased, the current I_D increases due to the flow of electrons from the source and these are pushed further due to the voltage applied at V_{GG}. Hence, the more positive the applied V_{GG}, the more the value of drain current I_D will be. The current flow gets enhanced due to the increase in electron flow better than in depletion mode. Hence this mode is termed as Enhanced Mode MOSFET.

Working of P Channel MOSFET:

When the gate terminal is given a negative potential at V_{GG} than the drain source voltage V_{DD}, then due to the P+ regions present, the holes current is increased through the diffused P channel and the PMOS works in Enhancement Mode.

When the gate terminal is given a positive potential at V_{GG} than the drain source voltage V_{DD}, then due to the repulsion, the depletion occurs due to which the flow of current reduces. Thus PMOS works in Depletion Mode. Though the construction differs, the working is similar in both the type of MOSFETs. Hence with the change in voltage polarity both of the types can be used in both the modes.

Drain Characteristics:

The drain characteristics of a MOSFET are drawn between the drain current I_D and the drain source voltage V_{DS}. The characteristic curve is as shown below for different values of inputs.

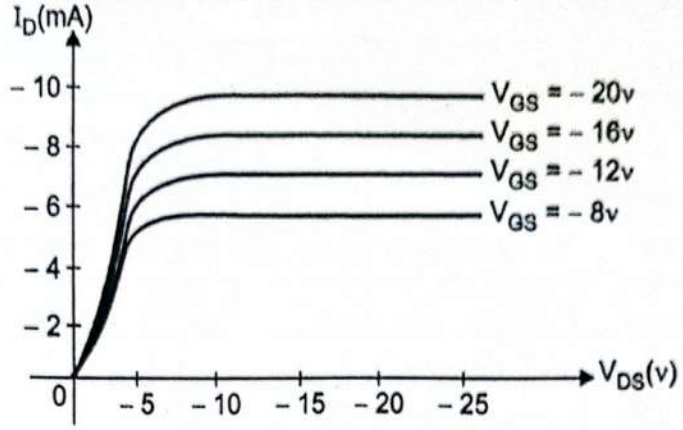


Fig. 5.21: Drain characteristics of MOSFET

Actually when V_{DS} is increased, the drain current I_D should increase, but due to the applied V_{GS}, the drain current is controlled at a certain level. Hence the gate current controls the output drain current.

Transfer Characteristics:

Transfer characteristics define the change in the value of V_{DS} with the change in I_D and V_{GS} in both depletion and enhancement modes. The below transfer characteristic curve is drawn for drain current versus gate to source voltage.

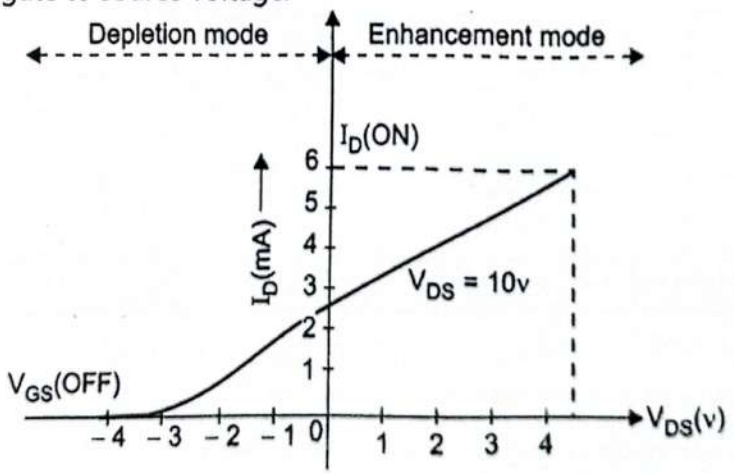


Fig. 5.22: Depletion and enhanced mode curves of MOSFET

Operating Regions of MOSFET:

Cutoff Region: In this region of the MOSFET, no current flows as the voltage applied in the MOSFET is less than the threshold voltage, resulting in the failure of the formation of the oxide layer. The state is OFF.

Saturation Region: In this region of the MOSFET, a constant amount of current flows between the drain and source because of the threshold voltage. State of MOSFET is ON in this case.

Triode Region: It is known as a partially conducting state. It is not fully turned on, but there is a channel for current flow. Voltage here is moderate.

Table 5.2: Switching Characteristics for Both N-channel and P-channel MOSFET

MOSFET	$V_{GS} < 0$	$V_{GS} = 0$	$V_{GS} > 0$
P-channel enhancement type	ON	OFF	OFF
N-channel enhancement type	OFF	OFF	ON
P-channel depletion type	ON	ON	OFF
N-channel depletion type	OFF	ON	ON

Table 5.3: Comparison between BJT, FET and MOSFET

TERMS	BJT	FET	MOSFET
Device type	Current controlled	Voltage controlled	Voltage Controlled
Current flow	Bipolar	Unipolar	Unipolar
Terminals	Not interchangeable	Interchangeable	Interchangeable
Operational modes	No modes	Depletion mode only	Both Enhancement and Depletion modes
Input impedance	Low	High	Very high
Output resistance	Moderate	Moderate	Low
Operational speed	Low	Moderate	High
Noise	High	Low	Low
Thermal stability	Low	Better	High

5.7 MODES OF MOSFET

Enhancement Type MOSFET

1. Drain Characteristics of Enhancement Type MOSFET

Characteristics between output current and output voltage.

O/P i –> I_D, O/P v –> V_{DS}, control variable = V_{GS}. Here we will plot a graph between I_D and V_{DS} for various levels of V_{GS}.

Case 1: $V_{GS1} > V_T$

(Here VT is the threshold voltage)

$$V_{eff} = V_{GS1} - V_T$$

Will directly affect the width of the n-channel

Significant amount of drain current will flow through it.

When V_{DS} is increased to a certain level, drain current becomes constant. This is called a pinch-off condition.

$$V_{DS} + V_{GD} - V_{GS} = 0$$

$$V_{GD} = V_{GS} - V_{DS}$$

$$V_{GD} = V_T, \text{ pinch off voltage}$$

Case 2: $V_{GS1} > V_{GS2}$

Conductivity of 1 > conductivity of 2

$$R_2 > R_1$$

Slope of 2 < slope of 1

Now there are few regions in this graph:

- **Saturation Region:** Region in which drain current is constant.
- **Triode Region:** Left area of locus of VDS saturation.
- **Cut-off Region:** When it can't achieve the threshold voltage, MOSFET remains OFF. Current is 0 amp.

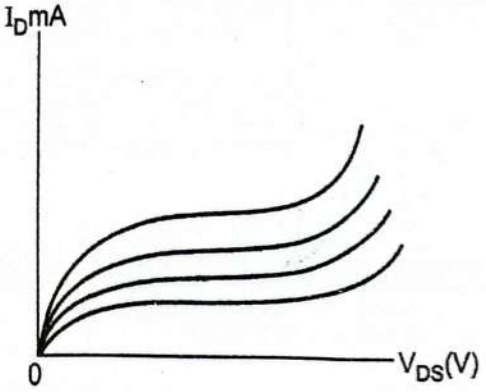


Fig. 5.23: Drain curves of MOSFET

With increasing voltage, current flowing through the terminals increases with voltage. we can see this in the graph. V_{GS} more than the threshold voltage is the condition of flowing current.

2. Transfer Characteristics of Enhancement Type MOSFET

Characteristics between output current and input voltage.

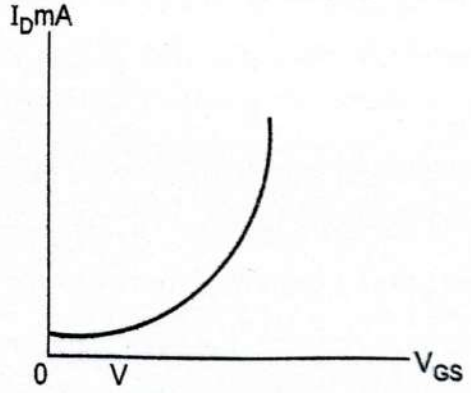


Fig. 5.24: Transfer characteristics of OSFET

When the value of voltage across gate and source is less than the threshold voltage

Working of N-Channel Enhancement Type MOSFET

In such a kind of MOSFET, we have to make the gate terminal more +ve, hence +ve charges will accumulate in the gate and will attract -ve charges in the body. Electrons_will be drifted towards the surface and the region near the surface will become less p type. +ve charges are pushed down. So the above region will become n type and thus a channel is formed. If we increase the voltage between gate and source, then the width of the channel will increase. If the voltage is more than a particular voltage, channel width is sufficient to allow the flow of current. This particular voltage is called Threshold voltage and the resultant current is known as drain current.

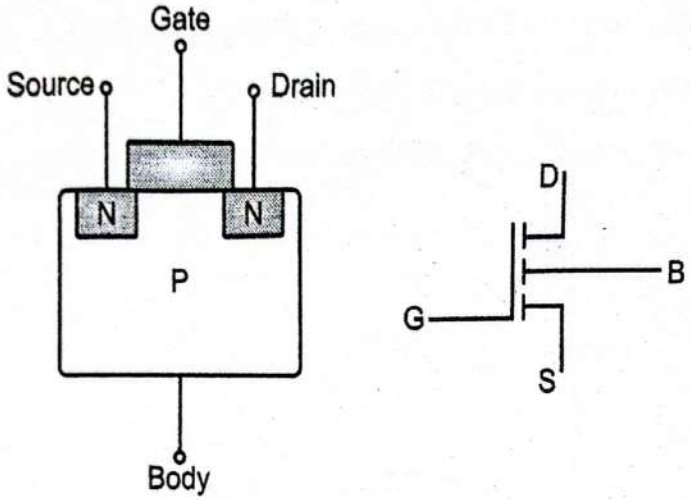


Fig. 5.25: MOSFET n type enhancement type

Working of P-Channel Enhancement Type MOSFET

A p-channel enhancement type MOSFET is a type of MOSFET that works by applying +ve voltage to the device. It operates according to the voltage applied to the gate terminal. Hence, the flow of current occurs between the drain and source. Step by step explanation:

- It has mainly three terminals, source, drain and gate. It forms on a semiconductor substrate.
- MOSFET has a thin insulating layer of oxide in it to separate it from the semiconductor. The source and drain terminals are made with p type semiconductors and so is the enhanced channel.
- In a p channel MOSFET, majority charge carriers are the holes.
- It is generally OFF when no voltage is applied. On applying voltage, it creates an electric field in the oxide layer and hence a channel is formed by the movement of holes.
- Then current starts flowing in the channel between drain and source.
- Substrate/body terminal is made up of n type semiconductor.
- Current in the channel can be controlled by gate voltage.

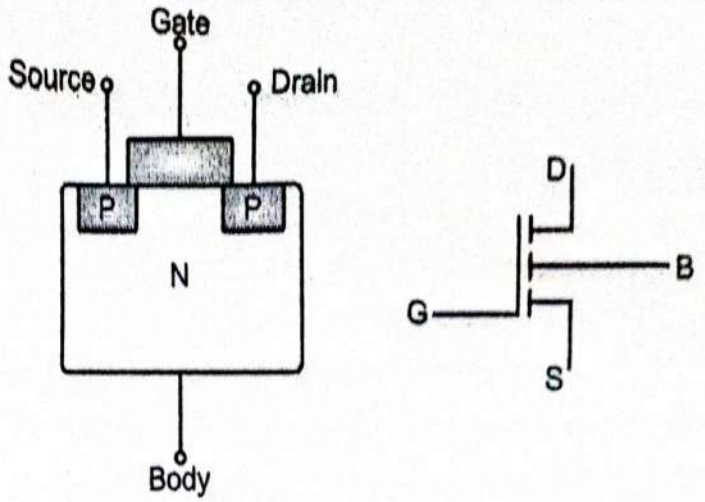


Fig. 5.26: MOSFET p type enhancement type

Working of N-channel Depletion Type MOSFET

- In this type of MOSFET, three terminals are present-drain, source and gate.
- Same as other MOSFETs, it also contains a thin insulating layer made up of gate oxide to avoid direct contact with the metal.
- Here, the channel is present from the beginning. By applying a +ve voltage, it creates a depletion region reducing the charge carriers and resulting in a decrement of current.
- MOSFET is generally ON.
- The drain and source terminal is made up of n-type semiconductor.

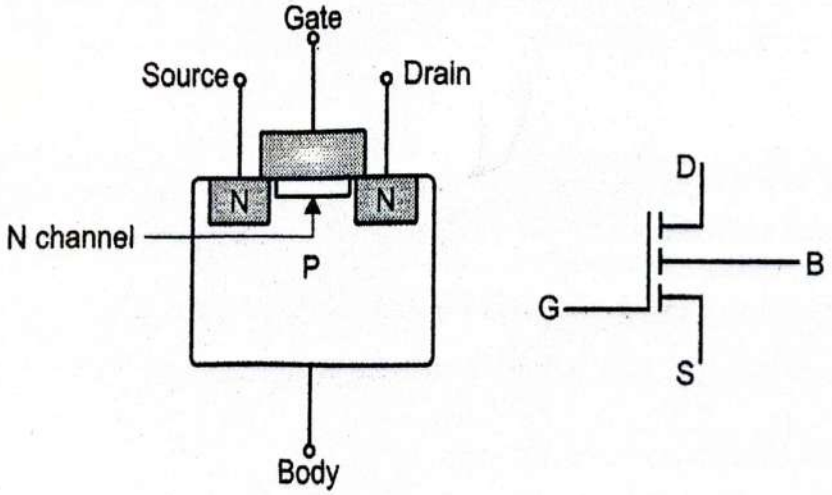


Fig. 5.27: MOSFET N channel depletion type

Working of P-channel Depletion Type MOSFET

- Like any other MOSFETs, this is also made with three main channels- drain, source and gate. Step by step explanation:
- Similar to other MOSFETs, there are mainly three terminals- gate, source and drain.
- The current between drain and source is controlled by the gate voltage but there is a difference. Channel is present from the beginning when no voltage is applied.
- Source and drain terminals are made with p type semiconductor and so is the channel. Majority charge carriers are the holes.

- Applying a -ve voltage, the channel depletes and hence the width of the channel decreases and hence the resistance increases decreasing the amount of current flowing.
- It is a voltage controlled resistor.

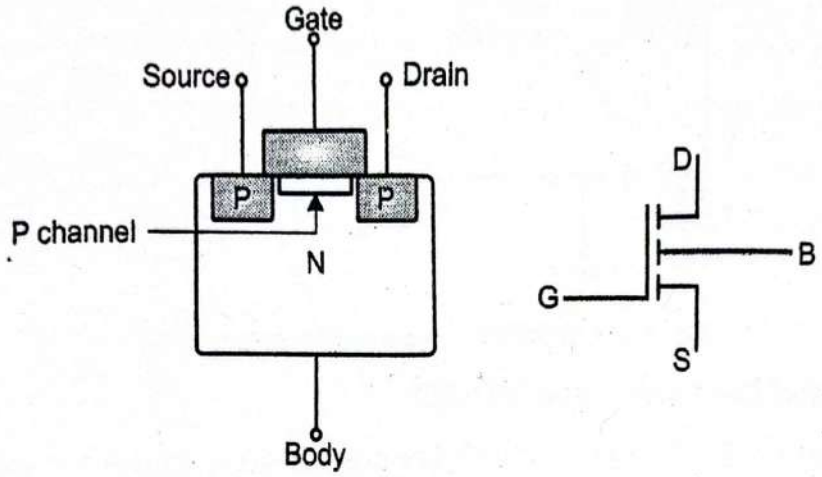
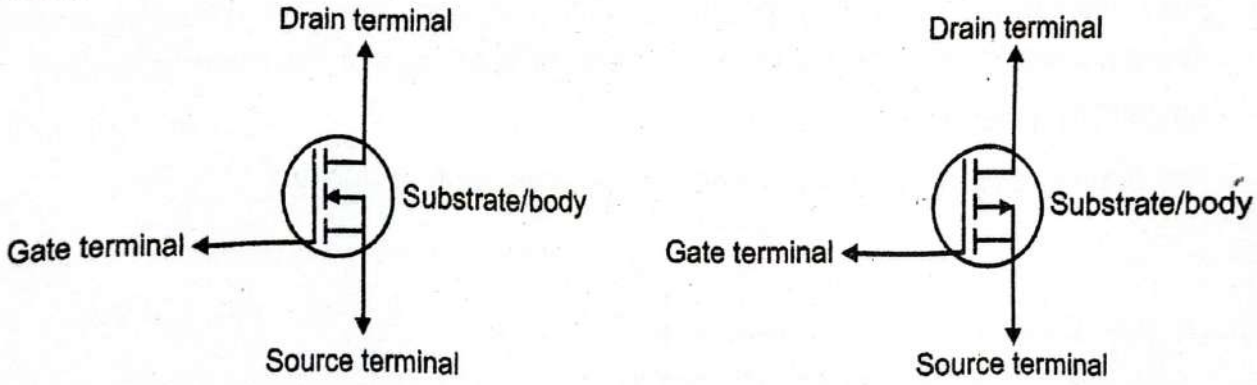


Fig. 5.28: MOSFET P channel depletion type

Symbols:



(a) N-channel enhancement **(b) P-channel enhancement**

Fig. 5.29: MOSFETs enhancement type

Depletion Type MOSFET:

Drain Characteristics: I_D Verses V_{DS} for various V_{GS}.

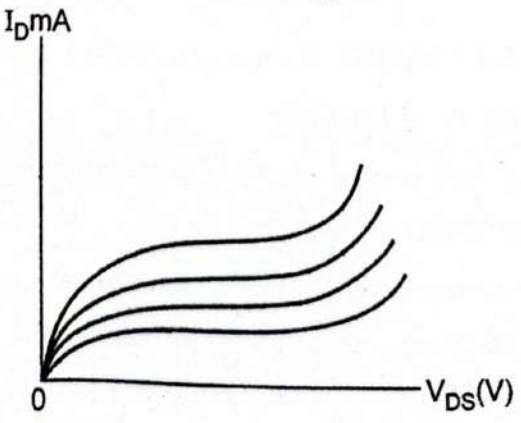


Fig. 5.30: Drain characteristics of MOSFET depletion type

Transfer Characteristics: I_D v/s V_{GS} for fixed V_{DS}.

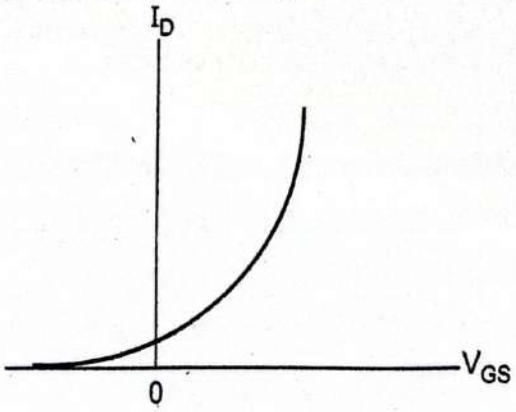
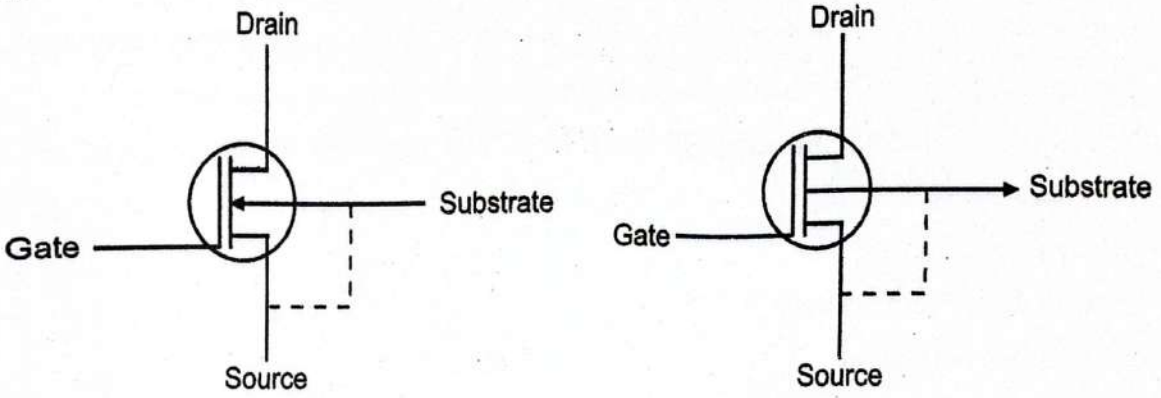


Fig. 5.31: Transfer characteristics of MOSFET depletion type

Symbols



(a) N-channel depletion type **(b) P-channel depletion type**

Fig. 5.32: MOSFETs depletion type

Table 5.4: Difference between Enhancement Type and Depletion Type MOSFET

Enhancement Type MOSFET	Depletion Type MOSFET
1. By applying external voltage in the channel, if the amount of charge carriers increases, it is known as enhancement type MOSFET.	1. By applying external voltage in the channel, if the amount of charge carriers decreases, it is known as depletion type MOSFET.
2. No channel is present in the beginning.	2. Channel is present from the beginning.
3. There is a threshold voltage.	3. There is no such threshold voltage.
4. It does not produce current in the absence of V_{GS}.	4. It can produce current without any gate voltage.

5.8 MOSFET APPLICATIONS AND THRESHOLD VOLTAGE

Applications of MOSFET

- **Amplifiers:** MOSFETs are used as an amplifiers in order to amplify weak signals.
- **Switching Power Supplies:** They are used as switches because they can alter power supply efficiently.

They are used to build logic gates such as NAND, NOR etc.

- **Voltage Regulators:** They are used as voltage regulators because they can control the amount of voltage.
- **Memory Devices:** They are used in memory cells.

Advantages of MOSFET

- **High Switching Speed:** It can change its state rapidly from ON and OFF position.
- **Low Power Consumption:** Useful for battery operated devices.
- **High Input Impedance:** They use minimum input current.
- **Low Noise:** They produce low noise and do not cause much disturbance.

Disadvantages of MOSFET

- **Breakdown:** MOSFETs have a very thin layer of gate oxide, so on applying high voltage, it can cause the breakdown of the entire device.
- **Temperature:** Some functions of MOSFET are altered because of varying temperatures.
- **Voltage Capacity:** They have a limited voltage capacity.
- **Expensive:** Complex manufacturing of MOSFETS can lead to high costs of overall electronic devices.

Uses of MOSFET

- Used in digital logic circuits.
- It is used as amplifiers.
- They are used in integrated circuits due to their small size.
- It is also used in microprocessors.
- Used in power electronics.

5.8.1 MOSFET as a Switch

P-channel MOSFET as a Switch:

We have looked at the N-channel MOSFET as a switch where the MOSFET is placed between the load and the ground. This also allows for the MOSFET's gate drive or switching signal to be referenced to ground (low-side switching).

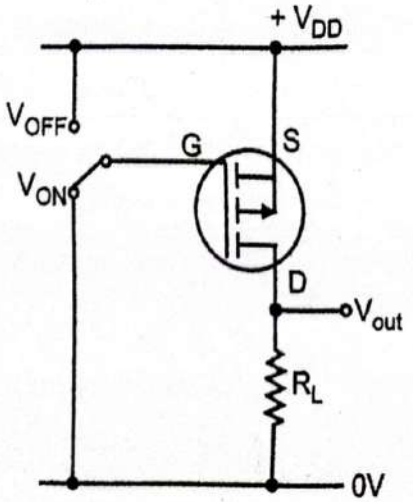


Fig. 5.33: P-channel: MOSFET switch

But in some applications we require the use of P-channel enhancement-mode MOSFET where the load is connected directly to ground. In this instance, the MOSFET switch is connected between the load and the positive supply rail (high-side switching) as we do with PNP transistors.

In a P-channel device, the conventional flow of drain current is in the negative direction so a negative gate-source voltage is applied to switch the transistor "ON".

This is achieved because the P-channel MOSFET is "upside down" with its source terminal tied to the positive supply $+V_{DD}$. Then when the switch goes LOW, the MOSFET turns "ON" and when the switch goes HIGH, the MOSFET turns "OFF".

This upside down connection of a P-channel enhancement mode MOSFET switch allows us to connect it in series with an N-channel enhancement mode MOSFET to produce a complementary or CMOS switching device as shown across a dual supply.

MOSFET as a Switch (Example)

If we understood the working of MOSFET and its regions of operation, we would have probably guessed how a MOSFET works as a switch. We understood the operation of a MOSFET as a switch by considering a simple example circuit.

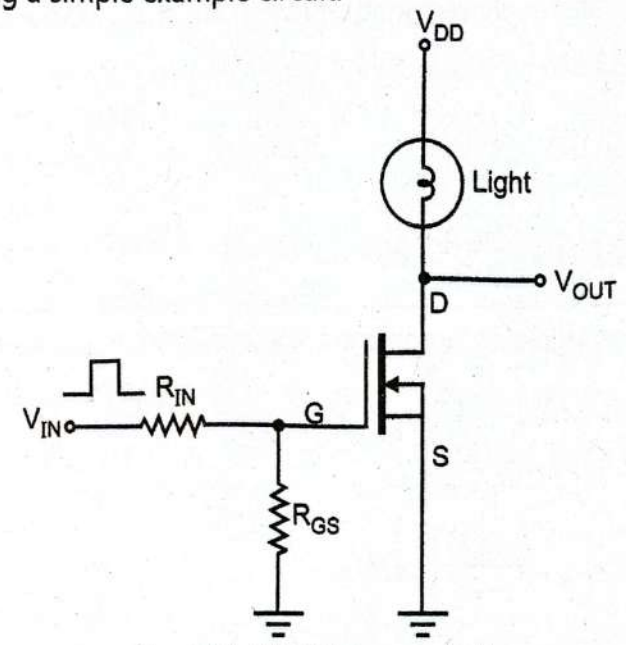


Fig. 5.34: MOSFET as a switch

This is a simple circuit, where an N-Channel enhancement mode MOSFET will turn ON or OFF a light. In order to operate a MOSFET as a switch, it must be operated in the cut-off and linear (or triode) region.

Assume the device is initially OFF. The voltage across Gate and Source i.e., V_{GS} is made appropriately positive (technically speaking, $V_{GS} > V_{TH}$), the MOSFET enters the linear region and the switch is ON. This makes the light to turn ON.

If the input gate voltage is 0V (or technically $< V_{TH}$), the MOSFET enters cut-off state and turns off. This in turn will make the light to turn OFF.

MOSFET as Capacitor:

MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) can be utilized as a component in a circuit that behaves like a capacitor, although it's not typically used for this purpose due to its primary function as a voltage-controlled switch. However, under certain conditions, the gate-source capacitance (Cgs) of a MOSFET can exhibit capacitor-like behavior.

5.9 NUMERICALS

Problem 5.1: *Fig. 5.35 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

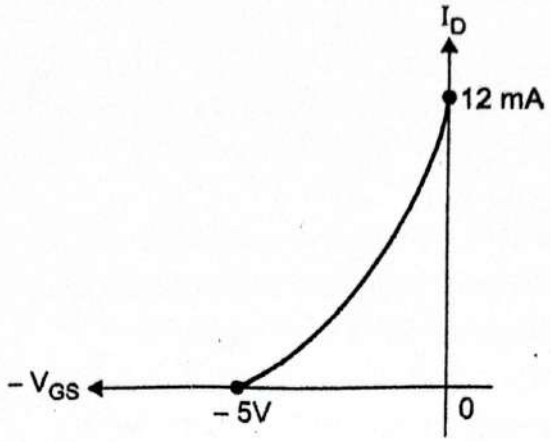


Fig. 5.35

Solution: Referring to the transfer characteristic curve in Fig. 5.35, we have,

$$I_{DSS} = 12 \text{ Ma} \quad , V_{GS(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$\text{or} \quad I_D = \mathbf{12}\left[\mathbf{1} + \frac{\mathbf{V_{GS}}}{\mathbf{5}}\right]^2 \textbf{ mA}$$

Problem 5.2: *A JFET has the following parameters: I_{DSS} = 32 mA; $V_{GS(off)}$ = – 8V; V_{GS} = – 4.5 V. Find the value of drain current.*

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

$$= \mathbf{6.12 \text{ mA}}$$

Problem 5.3: *A JFET has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS(off)}$ = – 6 V, find the value of (i) V_{GS} and (ii) V_P.*

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$\text{or} \quad 5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$\text{or} \quad 1 + \frac{V_{GS}}{6} = \sqrt{\frac{5}{10}} = 0.707$$

(i) $\therefore \quad V_{GS} = \mathbf{-1.76 \text{ V}}$

(ii) and $\quad V_P = -V_{GS(off)} = \mathbf{6 \text{ V}}$

Problem 5.4: *For the JFET in Fig. 5.36, $V_{GS(off)} = -4V$ and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

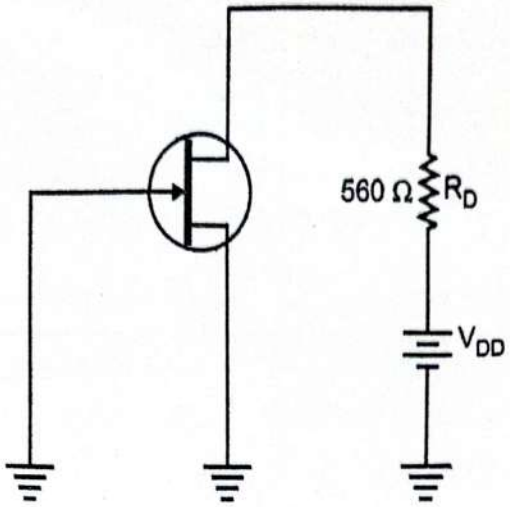


Fig. 5.36

Solution: Since $V_{GS(off)} = -4V$, $V_P = 4V$. The minimum value of V_{DS} for the JFET to be in constant-current region is

$$V_{DS} = V_P = 4V$$

In the constant current region with $V_{GS} = 0V$,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$

$$= 4V + (12 \text{ mA})(560\Omega) = 4V + 6.72V = \mathbf{10.72\ V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

Problem 5.5: *Determine the value of drain current for the circuit shown in Fig. 5.37.*

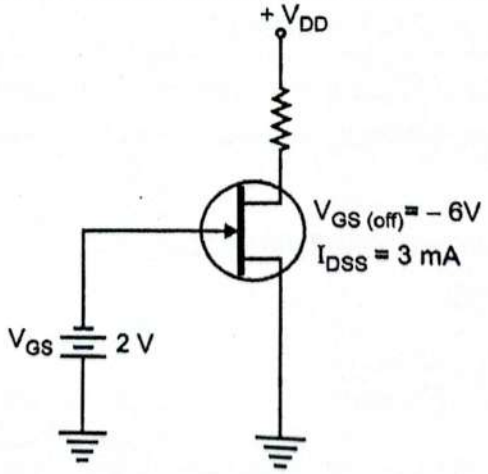


Fig. 5.37

Solution: It is clear from Fig. 5.37 that $V_{GS} = -2V$. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 3 \text{ mA}\left(1 - \frac{-2V}{-6V}\right)^2 = (3 \text{ mA})(0.444) = \mathbf{1.33\ mA}$$

Problem 5.6: *When a reverse gate voltage of 15 V is applied to a JFET, gate current is 10^{-3} μA. Find resistance between gate and source.*

Solution: $V_{GS} = 15\ V;\ I_G = 10^{-3}\ \mu A = 10^{-9}\ A$

$\therefore$ Gate to source resistance $= \dfrac{V_{GS}}{I_G}$

$$= \frac{15\ V}{10^{-9}\ A} = 15 \times 10^9\ \Omega$$

$$= \mathbf{15{,}000\ M\Omega}$$

Problem: 5.7: *When V_{GS} of JFET changes from –3.1 V to –3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance?*

Solution: $\Delta V_{GS} = 3.1 - 3 = 0.1\ V$

$$\Delta I_D = 1.3 - 1 = 0.3\ mA$$

$\therefore$ Transconductance,

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3\ mA}{0.1\ V} = 3\ mA/V = \mathbf{3000\ \mu\ mho}$$

Problem 5.8: *A JFET has a value of g_{mo} = 4000 μS. Determine the value of gm at $V_{GS} = -3V$. Given that $V_{GS(off)} = -8V$.*

Solution: $$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$= 4000\ \mu S\left(1 - \frac{-3V}{-8V}\right)$$

$$= 4000\ \mu S\ (0.625) = \mathbf{2500\ \mu S}$$

Problem 5.9: *The datasheet of a JFET gives the following information: I_{DSS} = 3 mA, $V_{GS(off)} = -6V$ and $g_{m\ (max)}$ = 5000 μS. Determine the transconductance for $V_{GS} = -4V$ and find drain current I_D at this point.*

Solution: At $V_{GS} = 0$, the value of g_m is maximum i.e. g_{mo}.

$\therefore$ $$g_{mo} = 5000\ \mu S$$

Now, $$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$= 5000\ \mu S\left(1 - \frac{-4V}{-6V}\right)$$

$$= 5000\ \mu S\ (1/3) = \mathbf{1667\ \mu S}$$

Also, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 3\ mA\left(1 - \frac{-4}{-6}\right)^2 = \mathbf{333\ \mu A}$$

Problem 5.10: *A JFET in Fig. 5.38 has values of $V_{GS(off)} = -8V$ and $I_{DSS} = 16$ mA. Determine the values of V_{GS}, I_D and V_{DS} for the circuit.*

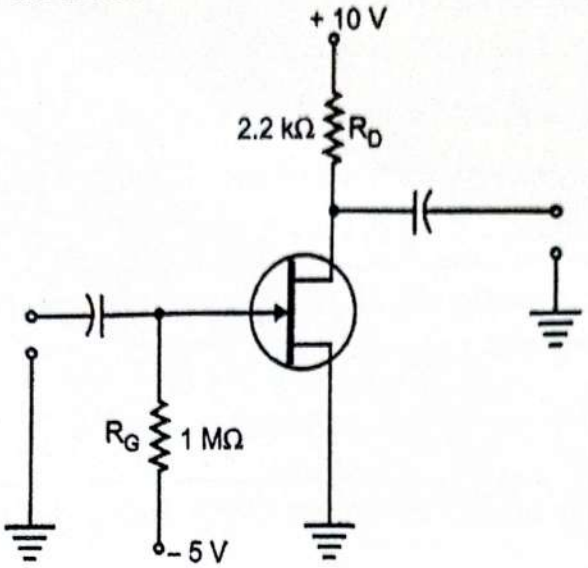


Fig. 5.38

Solution: Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \quad V_{GS} = V_{GG} = \mathbf{-5V}$$

Now,
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 16 \text{ mA}\left(1 - \frac{-5}{-8}\right)^2$$

$$= 16 \text{ mA } (0.1406) = \mathbf{2.25 \text{ mA}}$$

Also,
$$V_{DS} = V_{DD} - I_D R_D$$

$$= 10 \text{ V} - 2.25 \text{ mA} \times 2.2 \text{ k}\Omega = \mathbf{5.05 \text{ V}}$$

Note that operating point for the circuit is 5.05 V, 2.25 mA

Problem 5.11: *Find V_{DS} and V_{GS} in Fig. 5.39, given that $I_D = 5$ mA.*

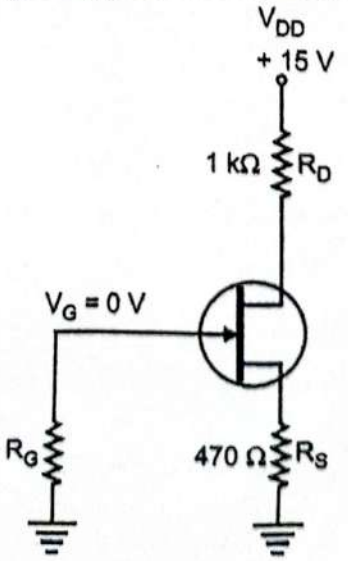


Fig. 5.39

Solution: $V_S = I_D R_S = (5\text{ mA})(470\ \Omega) = 2.35\text{ V}$

and $V_D = V_{DD} - I_D R_D$

$= 15\text{V} - (5\text{ mA}) \times (1\text{ k}\Omega) = 10\text{ V}$

$\therefore$ $V_{DS} = V_D - V_S = 10\text{ V} - 2.35\text{ V} = \mathbf{7.65\ V}$

Since there is no gate current, there will be no voltage drop across R_G and $V_G = 0$.

Now, $V_{GS} = V_G - V_S = 0 - 2.35\text{ V} = \mathbf{-2.35\ V}$

Problem 5.12: *The transfer characteristic of a JFET reveals that when $V_{GS} = -5V$, $I_D = 6.25\ mA$. Determine the value of RS required.*

Solution: $R_S = \dfrac{|V_{GS}|}{|I_D|} = \dfrac{5\text{V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$

Problem 5.13: *Determine the value of R_S required to self-bias a p-channel JFET with $I_{DSS} = 25\ mA$, $V_{GS(off)} = 15\ V$ and $V_{GS} = 5V$.*

Solution:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = 25\text{ mA}\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2 = 25\text{ mA}\,(1 - 0.333)^2 = 11.1\text{ mA}$$

$\therefore$ $R_S = \dfrac{|V_{GS}|}{|I_D|} = \dfrac{5\text{V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$

Problem 5.14: *Draw the D.C. load line for the JFET amplifier shown in Fig. 5.40.*

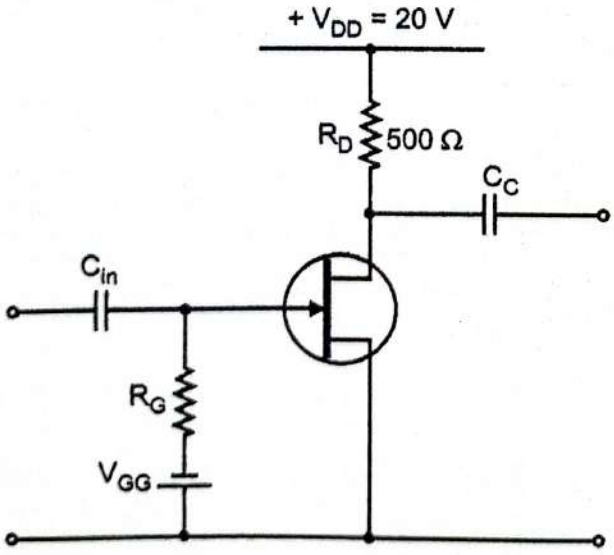


Fig. 5.40

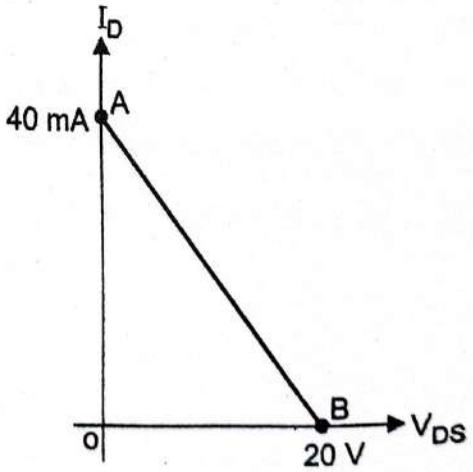


Fig. 5.41

Solution: Max. $V_{DS} = V_{DD} = 20\text{ V}$

This locates the point B (OB = 20V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D} = \frac{20\text{ V}}{500\ \Omega} = 40\text{ mA}$$

This locates the point A (OA = 40 mA) of d.c. load line.

Fig. 5.41 shows the D.C. load line AB.

QUESTIONS

1. With relevant diagrams and characteristic curves, explain the operation of JFET.
2. Draw the drain and transfer characteristics of n-channel JFET and explain.
3. Explain the construction of an N channel JFET. Also explain drain and transfer characteristics
4. Explain three distinct regions of the output characteristics.
5. Define the pinch-off voltage of JFET.
6. Draw the drain characteristics of FET and indicate important operating regions.
7. State any two advantages of FET over BJT.
8. State any four applications of FET
9. Define intrinsic stand-off ratio.
10. Define
    (i) I_{DSS}
    (ii) V_{GS} (cut off)
11. What is meant by Pinch-off voltage?
12. Define amplification factor.
13. Draw the symbol of n-channel JFETs and P-channel JFETs.
14. Draw Drain Characteristics of JFET
15. Draw the transfer characteristics of JFET.
16. Define parameters of FET
    (i) A.C. drain resistance
    (ii) D.C. drain resistance
17. Define parameters of FET
    (i) Trans conductance
    (ii) Amplification factor
18. Comment "FET is a unipolar device while BJT is a bipolar device."
19. Comment "The input Impedance of FET amplifier is higher than that of a BJT amplifier"
20. What are the parameters of JFET?
21. Why is the noise level in FET is smaller than in BJT?
22. Define drain resistance and Transconductance.
23. Define Transconductance and amplification factor of FET.
24. Give the relationship between different JFET parameters?
25. Compare P-channel JFET with N-channel JFET.
26. Compare FET and BJT.
27. Compare FET and MOSFET.
28. What are the differences between BJT and JFET?
29. What are the applications of JFET?

30. Define the threshold voltage of a MOSFET
31. What are the differences between JFETs and MOSFETs?
32. What precautions are to be taken when handling MOSFET?
33. Depletion MOSFET is commonly known as "Normally-on" MOSFET. Why?
34. State specification parameters for JFET and MOSFET.
35. Compare N channel MOSFETs with P-channel MOSFETs.
36. Draw symbol
    (i) P-channel depletion MOSFET
    (ii) N-channel depletion MOSFET
37. Draw and explain the characteristics of JFET.
38. Explain FET as a Voltage Variable Resistor.
39. Explain JFET as a switch.
40. Explain the working of a P channel JFET and draw its V-I characteristics.
41. Explain the working of an N channel JFET and draw its V-I characteristics.
42. Why is the input impedance in FET very high in comparison with BJT?
43. Why is FET preferred as a Buffer Amplifier?
44. In an n-channel JFET, I_{DSS} = 20 mA and V_P = – 6V. Calculate the drain current when V_{GS} = – 3V.
45. Determine the trans-conductance of a JFET. If its amplification factor is 96 and drain resistance is 32 KΩ.
46. Define and explain the three parameters of a JFET and give the relation between them.
47. Explain with the help of neat diagrams, the structure of an N-channel FET and its Volt-ampere characteristics. In what ways is it different from a bipolar transistor.
48. Explain working of depletion mode MOSFET with circuit diagram.
49. Explain working of Enhancement mode MOSFET with circuit diagram.
50. What is the major difference in the construction of the D-MOSFET and E-MOSFET.
51. Draw the transfer characteristics for JFET and N-Channel MOSFET.
52. Explain MOSFET as a switch.
53. What is the major difference in the construction of the D-MOSFET and the E-MOSFET?
54. Draw the transfer characteristics for JFET and N-Channel MOSFET.
55. Describe the kind of operation that takes place in an enhancement mode MOSFET. How does this differ from depletion mode?
56. Describe construction and explain the operation of depletion mode MOSFET. Also draw the static characteristics.

Module - VI

NANOTECHNOLOGY

Syllabus:

- *Introduction to Nanotechnology, Properties (optical, Electrical, Structural, Mechanical,) Importance of surface to Volume ratio, bonding in solids (Vander walls interactions), Application: Lithography, Single Electron Transfer (SET) and Spin Valves.*

Objectives:

- *To give exposure to the upcoming field of Nano technology in the field of solid state physics.*

Outcome:

- *Learner will be able to Apply the knowledge of Nano Technology to certain emerging areas of technology.*

List of Contents:

6.1 Introduction to Nanotechnology

6.1.1 Nano Material

6.1.2 Classification of Nanomaterials

6.1.3 Synthesis of Nanomaterials

6.2 Properties (Optical, Electrical, Structural, Mechanical) of Nanomaterials

6.2.1 Optical Properties of Nanoparticles

6.2.2 Magnetic Properties of Nanoparticles

6.2.3 Electrical Properties of Nanoparticles

6.2.4 Electronic and Structural Properties of Nanoparticles

6.2.5 Mechanical Properties of Nanoparticles

6.3 Importance of Surface to Volume Ratio

6.4 Bonding in Solids (Vander Walls Interactions)

6.4.1 Van der Waals Forces

6.4.2 Properties of Van der Waals Forces

6.4.3 Types of Van der Waals Forces

6.4.4 Factors Affecting Van der Waal Forces

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6.5 Applications of Nanotechnology
6.5.1 Lithography and its Types
6.5.2 Single Electron Transfer (SET)
6.5.3 Spin Valves
- *Questions*

6.1 INTRODUCTION TO NANOTECHNOLOGY

Nanotechnology is the manipulation of matter on an atomic or molecular scale, typically between 1 and 100 nanometers. At this scale, materials exhibit unique physical and chemical properties due to quantum mechanical effects and a high surface area to volume ratio. This field encompasses various scientific disciplines, including physics, chemistry, biology and engineering and aims to create new materials and devices with enhanced capabilities. Nanotechnology is the *science and engineering of functional systems at the molecular scale.* In its original sense, nanotechnology refers to the projected ability to construct items from the bottom up making complete, high-performance products.

The history of nanotechnology traces back to ancient times when artisans unknowingly used nanoparticles in pottery and glass. Richard Feynman 1959 lecture, *there is Plenty of Room at the Bottom* and is often credited with inspiring the field by discussing the potential of manipulating atoms and molecules. Norio Taniguchi first coined the term nanotechnology in 1974 and describing processes that operate on a nanometer scale.

The field gained significant momentum in 1980s with the invention of the *scanning tunneling microscope* and the discovery of fullerenes. K. Eric Drexler further popularized nanotechnology in the 1980s through his book and Engines of Creation and which envisioned molecular machines capable of self-replication. Industrial revolution has made life easy and pleasant. Today's high speed personal computers and mobile communications would not have certainly been possible without the use of nano science and nano technology.

6.1.1 Nano Material

Nanoscale materials are defined as a set of substances where at least one dimension is less than approximately 100 nanometers. A nanometer is one millionth (10^{-9}m) of a millimeter that is approximately 100,000 times smaller than the diameter of a human hair. Nanomaterials are of interest because at this scale unique optical, magnetic, electrical and other properties emerge. These emergent properties have the potential for great impacts in electronics, medicine and other fields. They contain a very large number of grain boundaries, which increases their properties. They exhibit different properties such as tremendous strength, hardness, formability and toughness.

Nanomaterials have an extremely small size which having at least one dimension 100 nm or less. Nanomaterials can be nanoscale in one dimension (Ex. surface films), two dimensions (Ex. strands or fibres) or three dimensions (Ex. Particles). They can exist in single, fused, aggregated or agglomerated forms with spherical, tubular and irregular shapes. Common types of nanomaterials include nanotubes, dendrimers, quantum dots and fullerenes. Nanomaterials have applications in the field of nano technology and displays different physical chemical characteristics from normal chemicals (i.e., silver nano, carbon nanotube, fullerene, photo catalyst, carbon nano and silica).

Different Forms of Nanomaterials:

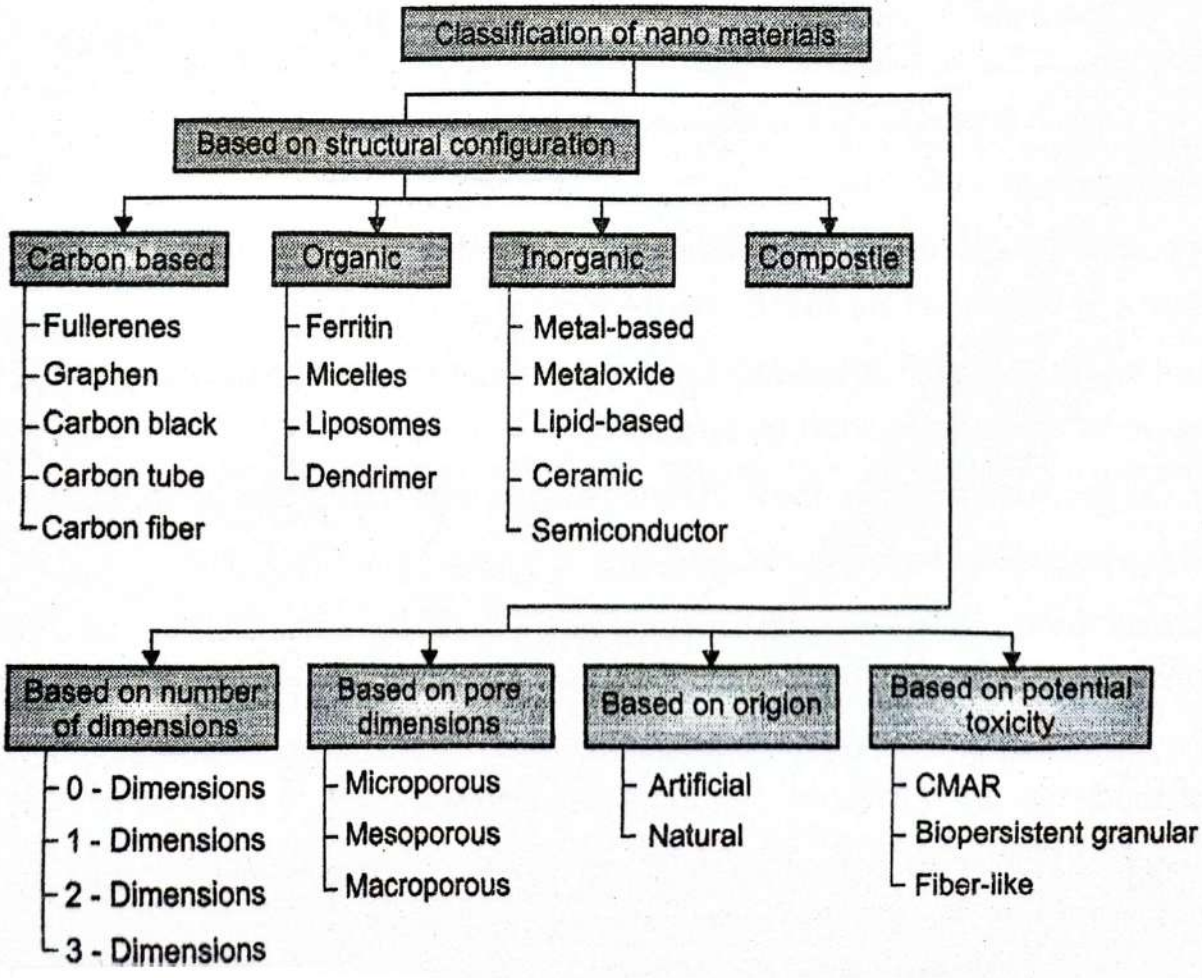
1. Nano particles
2. Nano dots
3. Nano rods
4. Nano tubes
5. Nanowires
6. Fullerenes
7. Nanocomposites
8. Cluster
9. Colloids

6.1.2 Classification of Nanomaterials

Natural and artificial nanoparticles are the two groups into which nanomaterials are divided based on origin.

(a) Natural Nanomaterials: Natural nanomaterials can be found in a variety of forms in nature, including viruses, protein molecules, minerals like clay, natural colloids like milk and blood (liquid colloids), fog (aerosol type), gelatin (gel type), mineralized natural materials like shells, corals and bones, insect wings and opals, spider silk, lotus leaves, gecko feet, volcanic ash and ocean spray.

(b) Artificial Nanomaterials: Carbon nanotubes and semiconductor nanoparticles like quantum dots are the examples of artificial nanomaterials that are made consciously using precise mechanical and manufacturing procedures. Nanomaterials are categorized as metal based materials, dendrimers or composites depending on their structural makeup.



6.1.3 Synthesis of Nanomaterials

Nanomaterials are broadly synthesized by Top down and bottom up approaches.

Top Down Approach

- A top-down approach where very small structures are produced from larger (Bulk) pieces of material.
- It includes slicing or successive cutting of a bulk material to get nanosized particles.
- Synthesis of nanomaterials on a large scale production can be easily done.
- Chemical purification is not required.
- It is an expensive method where deposition parameters cannot be controlled. The particles of different sizes are obtained and impurities can be introduced during synthesis.
- For example, Ball milling (Mechanical alloying) method, electrochemical etching and Photo-Lithography.

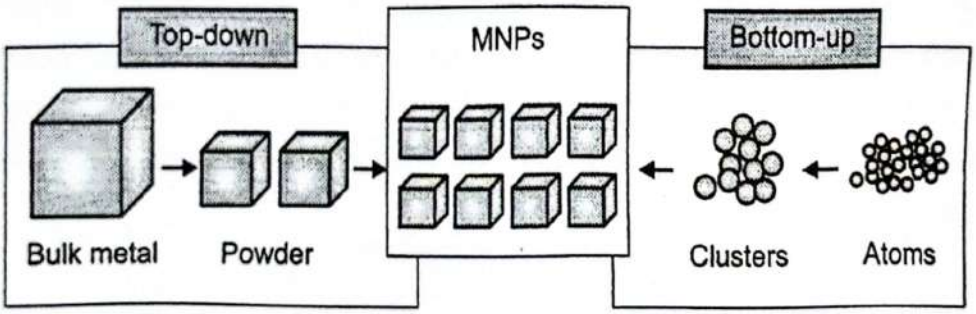


Fig. 6.2: Synthesis of nanomaterials by top down and bottom up approach

Bottom up Approach

- A bottom-up approach can be viewed as a synthesis approach where the building blocks (atoms or molecules) are added onto the substrate to form the nanostructures.
- Bottom-up approach is building up of a material from the bottom i.e., atom by atom, molecule by molecule or cluster by cluster.
- In this approach of the synthesis of nanomaterials large scale production is difficult.
- Chemical purification is required.
- It is comparatively less expensive method where deposition parameters can be controlled. Ultra-fine Particles are obtained and impurities are not introduced during the synthesis.
- For example, Chemical Vapor deposition method, Physical Vapor Deposition and Sol Gel method.

Both approaches play an important role in the synthesis of nanomaterials. Various synthesis methods of Nanomaterials are (i) Ball milling or Mechanical grinding (ii) Pulsed Laser Deposition (iii) Chemical vapor deposition (iv) Sol Gel method (v) Electro-deposition, etc.

6.2 PROPERTIES (OPTICAL, ELECTRICAL, STRUCTURAL, MECHANICAL) OF NANOPARTICLES

Due to their small size, nanomaterials have special optical, magnetic, electrical and physical, reactivity, strength, surface area, sensitivity and stability features.

6.2.1 Optical Properties of Nanoparticles

Because of the quantum confinement in nanomaterials, the emission of visible light can be tuned by varying the nanoscale dimensions. It is observed that the size reduction in nanomaterials shifts the emission of peak towards the shorter wavelength (blue shift).

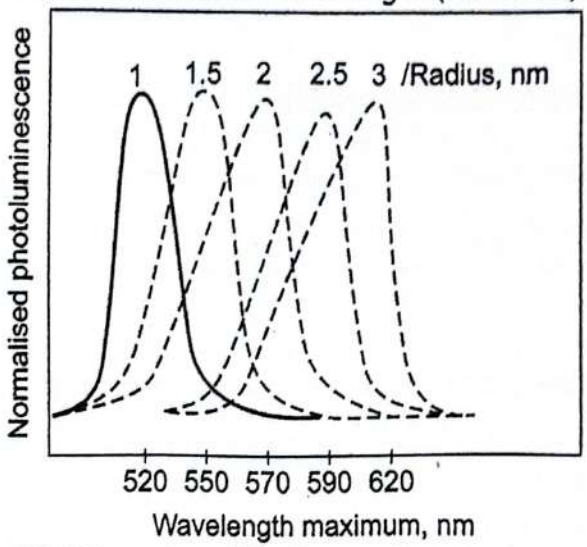


Fig. 6.3: Effect of particle size on photoluminescence

6.2.2 Magnetic Properties of Nanoparticles

Magnetic nanoparticles are those which can be affected using a magnetic field. These particles usually contain magnetic elements like iron, nickel, cobalt etc. Magnetic nanoparticles show a variety of unusual magnetic behavior when compared to the bulk materials, mostly due to surface or interface effects, including symmetry breaking, electronic environment or charge transfer and magnetic interactions.

Magnetic Properties of Nanomaterials with Examples

- The physical and chemical properties of magnetic nanoparticles mainly depend upon the chemical structure and method of synthesis. For example, nano scale particles of magnetite show superparamagnetism at a transition temperature, which is smaller than the transition temperature of bulk material.
- Nanocomposite magnets consisting of a uniform mixture of magnetically hard and soft phases have been extensively investigated in recent years due to their useful hard magnetic properties.
- High energy products and relatively high coercivities can be developed in these nanocomposite magnets. These magnets have a high value of remanence and low cost.
- Magnetic studies in nanostructured materials have focused on the interaction between electron charges and magnetic spins and these studies have led to discoveries of new and unique phenomena that are neither observable in traditional bulk materials, nor explainable using classical theories. For examples: Giant Magnetoresistance (GMR) in multilayers and metallic granular solids, spin valves, spin injection etc.

- Magnetostrictive materials are of great scientific importance to us. Magnetostriction is the process in which magnetic material is deformed due to the presence of a magnetic field.
- Magneto restrictive nano scale films can allow such functions, which cannot be done using existing integrated circuits. For example these constitute driving elements of micro robots, pumps, motors, etc. These can also be used for magnetic control of elastic properties or dependence of stress or strain on magnetic permeability to develop various electronic devices like a resonator with magnetically adjustable frequency and stress controlled inductance.

6.2.3 Electrical Properties of Nanoparticles

The large grain boundary (surface) area of nanomaterials allows them to store far more energy than typical coarse-grained materials. The passage of an electric current through these materials or the application of an electric field can introduce a new optical absorption band or modify an existing band.

Many devices that require electrical power make use of both standard and rechargeable batteries. These batteries typically have a low energy density (storage capacity), necessitating frequent recharge. Because they are able to store far more energy than traditional ones, nanocrystalline materials are promising candidates for use as separator plates in batteries. It is expected that nickel-metal hydride batteries, which combine nanocrystalline nickel with metal hydrides, will last significantly longer and need charging a lot less frequently. Moreover, the dielectric properties are significantly enhanced by making these nanocrystalline.

In general, nanomaterials are inferior to bulk materials in terms of thermal and electrical conductivity. According to the classical free electron theory of metals, electrical conductivity results from the free movement of electrons within a metallic solid. High electric-phonon and phonon-phonon scattering in nanomaterials is responsible for their low conductivity.

6.2.4 Electronic and Structural Properties of Nanoparticles

It is a material with any external dimension in the nanoscale or having internal structure or surface structure in the nanoscale. Nanomaterial exhibits unique microstructure and enhanced mechanical performance. In bulk materials, conduction of electrons is delocalized, that is, electrons can move freely in all directions. When the scale is reduced to nanoscale, the quantum effect dominates. For zero dimensional nanomaterials, all the dimensions are at the nanoscale and hence the electrons are confined in 3-D space. Therefore, no electron delocalization (freedom to move) occurs. For one dimensional nanomaterials, electron confinement occurs in 2-D space and hence electron delocalization takes place along the axis of nanotubes/Nano rods/nanowires. Due to electron confinement, the energy bands are replaced by discrete energy states, which make the conducting materials to behave like either semiconductors or insulators.

6.2.5 Mechanical Properties of Nanoparticles

Due to the essentially unique properties that nanocrystalline materials exhibit, there has been a lot of research done on the mechanical behavior of these materials. Because of the complex interaction of the defect structures, the tensile, work hardening, creep, fatigue and deformation behaviors of nanocrystalline materials are very different from those of their bulk counterparts. This is owing to the fact that nanocrystalline materials are much smaller.

The following is a list of the main factors that contribute to the significant differences in the mechanical behavior of nanostructured materials

- The behavior of these defects in response to the application of stress is strongly impacted by the presence of a very high fraction of the atoms that reside at grain boundaries and triple junctions. The effect that grain size has on the stability of dislocations also has a substantial impact on the dynamics of dislocations, which in turn has repercussions for both the design of materials and their mechanical properties. Because dislocation interactions are the major deformation processes that determine the mechanical properties of coarse-grained materials, the plastic deformation mode of nanomaterials may be drastically different. This is because dislocation interactions are responsible for determining the mechanical properties of coarse-grained materials.
- Alternate deformation mechanisms such as grain boundary migration or sliding, crack expansion and other similar processes become relevant for the reasons mentioned above.
- The amount of porosity in nanomaterials is significantly dependent on the processing technique that was used and this porosity level can also be substantial, for instance in the case of specimens that were mechanically alloyed. Even after agglomeration, the pore size may still be less than the grain size or even the same. It's possible that the presence of porosity will have a substantial impact on the way nanomaterials behave mechanically.
- Also, the mechanical characteristics of nanomaterials may be affected by the segregation of various solutes at the grain boundaries.

The greater density of defects such as grain boundaries, dislocations, triple junctions, etc., is what gives nanomaterials their distinctive mechanical properties due to the increased number of surface atoms and interfaces. When compared to bulk materials, nanomaterials have the following mechanical properties:

- Increased strength
- Increased toughness
- Increased hardness
- Increased ductility

6.3 IMPORTANCE OF SURFACE TO VOLUME RATIO

The surface-to-volume ratio plays a crucial role in determining the properties of materials at the nanoscale. As materials decrease in size, their surface area increases relative to their volume, leading to enhanced reactivity, strength and electrical conductivity.

Surface area to volume ratio in nanoparticles has a significant effect on the nanoparticles properties. Firstly, nanoparticles have a relatively larger surface area when compared to the same volume of the material. For example, let us consider a sphere of radius (r).

The surface area of the sphere will be $4\pi r^2$

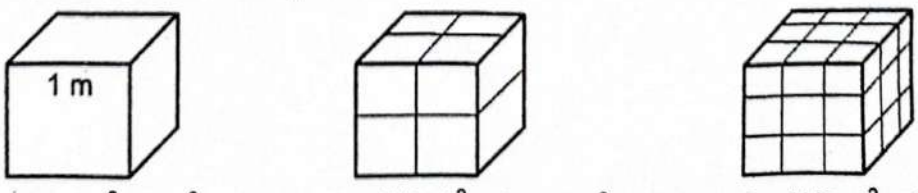
The volume of the sphere = $\frac{4}{3}\pi r^3$

Therefore, the surface area to the volume ratio will be $\frac{4\pi r^2}{\left\{\frac{4\pi r^3}{3}\right\}} = \frac{3}{r}$

It means that the surface area to volume ratio increases with the decrease in radius of the sphere and vice versa. It can also be conclude here that when a given volume is divided into smaller pieces, the surface area increases. Therefore, as particle size decreases, a greater portion of the atoms are found at the surface compared to those inside.

For Example: A particle of size 3 nm has 50% of its atoms on its surface, at 10 nm 20% of its atoms and at 30 nm has 5% of its atoms on its surface. Therefore, nanoparticles have a much greater surface area per unit volume compared with the larger particles. It leads to nanoparticles that are more chemically reactive. As growth and catalytic chemical reaction occurs at surfaces, therefore a given mass of nanomaterial will be much more reactive than the same mass of material made up of large particles. It is also found that materials that are inert in their bulk form are reactive when produced in their nanoscale form. It can improve their properties.

The smaller the radius/size of any material, higher the surface area. Thus nanoparticles have a much greater surface area as compared with larger particles. It makes materials more chemically reactive. This affects their strength or electrical properties hence they are used mainly in sensors. A characterization parameter for the effectiveness of a nanoparticle is the ratio of its surface area to its volume. Explain with an example of a cube.



Area = 6 x $1m^2$ = $6m^2$ Area = 6 x $(1/2m)^2$ x 8 = $12m^2$ Area = 6 x $(1/3m)^2$ x 27 = $18m^2$

Fig. 6.4

Let us consider an example. For a one cubic volume shown in Fig. 6.4, the surface area is $6m^2$. When it is divided into eight pieces, its surface area becomes $12m^2$. When the same volume is divided into 27 pieces its surface area becomes $18m^2$. Thus when the given volume is divided into smaller pieces, the surface area increases. Hence, as particle size decreases, a greater proportion of atoms are found at the surface compared to those inside. Thus nanoparticles have a much greater surface area compared with larger particles.

Quantum Confinement Effect:

In the bulk matter, the bands are actually formed by the merger of adjacent energy levels of a large number of atoms and molecules. As the particle size reaches the nano scale, the number of overlapping orbitals or energy levels decreases and the width of the band gets narrower. This will cause an increase in the energy gap between the valence band and the conduction band. Therefore, there is a higher energy gap in nanoparticles than the 10 corresponding bulk materials. The band gap is the region forbidden for the electrons. The larger the forbidden region, the greater will be restriction on the movement of electrons. The electrons are thus confined in space and are not free to move. This effect is thus called quantum confinement. *This affects the optical, electrical and magnetic behavior of materials at nano scale.*

6.4 BONDING IN SOLIDS (VANDER WALLS INTERACTIONS)

Van der Waals forces, also known as Van der Waals bonds or Van der Waals interaction, are weak intermolecular interactions observed in condensed phases like solid and liquid. They are responsible for the bulk properties of substances, like the boiling and melting points. Van der Waals bonds are secondary bonds in molecules where ionic and covalent bonds form the primary bonds.

6.4.1 Van der Waals Forces

When two atoms are close to each other, there are attractive and repulsive forces called Van der Waal forces, which depend on their distance of separation from each other. The combined force is given by the equation

$$F_{(R)} = \frac{A}{R_r^x} - \frac{B}{R_r^y}$$

Where, F = resultant force between the atoms

R = distance between the two atoms

r = unit vector along the line joining the two atoms

A, B, x, y are constants

The first term in the equation is the repulsive force and the second term is attractive force between the two atoms. The repulsive force is more effective at very short distance and changes rapidly with distance. This is due to the repulsive interaction between the electron clouds at a short distance (Pauli's exclusion principle).

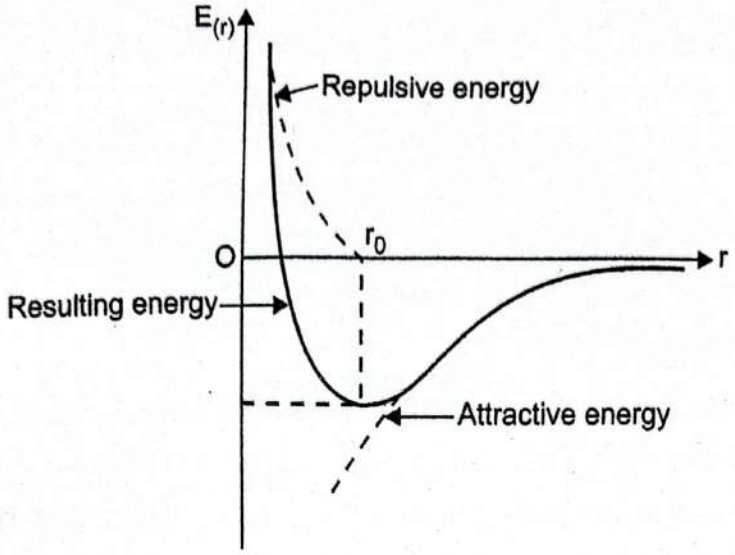


Fig. 6.5: Van der Waals forces

Molecules bounded together by Van der Waals forces occur due to the fluctuations in the charge density of particles. As a result, an atom or molecule is polarized with positive charges at one end and negative charges at the other end. The polarization gives rise to electrostatic forces between the two atoms or molecules. These weak forces are responsible for holding the atoms or molecules together. Van der Waals forces disappear as the distances between the atoms or molecules increase.

Van der Waals radius is the radius of an imaginary sphere surrounding an atom. It represents the distance of the closest approach for another atom. In other words, Van der Waals radius is one half of the distance of separation between the centers of the two approaching nuclei. It is a parameter that determines whether the atoms or molecules will hold together in a solid or liquid.

Van der Waals interaction is a ubiquitous but subtle force between particles mediated by quantum fluctuations of charge. It is the most long-range force acting between particles and influences a range of phenomena such as surface adhesion, friction and colloid stability.

6.4.2 Properties of Van der Waals Forces

Some characteristics of the Van der Waals forces are as

- Additive, i.e., several intermolecular interactive forces add together to form a quantifiable force.
- Non-directional, i.e., they can attract atoms or molecules from all directions.
- Weaker than ionic and covalent chemical bonds.
- Act only over a short range. The interaction is significant when molecules are positioned closer.
- Independent of temperature, except dipole-dipole interactions.

6.4.3 Types of Van der Waals Forces

There are two types of Van der Waals forces:

1. **London Dispersion Forces:** London dispersion forces are intermolecular forces that occur between two atoms or two nonpolar molecules due to the motion of electrons. An atom consists of a nucleus and electrons that move in orbits. At any time, the electrons can cluster around one part of the atom. As a result, the atom becomes negatively charged at one end and positively charged at the other end, resulting in an instantaneous dipole. This weak and temporary dipole then influences neighboring atoms through electrostatic attraction and repulsion, thereby inducing dipoles. The induced dipoles are feebly attracted to one another. The strength of dispersion forces increases as the number of electrons in the atoms or nonpolar molecules increases. These forces are named after Fritz London, who first proposed their existence in 1930.

   Example: Helium (He), chlorine (Cl_2) and carbon tetrachloride (CCl_4).

2. **Dipole-Dipole Interactions:** The dipole-dipole interactions or dipole-dipole forces arise because of the electric polarization induced particles due to the presence of other particles. They are similar to London Dispersion forces, but they occur in molecules that have a permanent dipole. Here, the negative end of a polar molecule attracts the positive end of another polar molecule. This attraction between these two molecules is known as the dipole-dipole force. Hydrogen bonding is a particular type of dipole-dipole interaction.

   Examples: Water (H_2O) and hydrogen chloride (HCl).

6.4.4 Factors Affecting Van der Waal Forces

Two factors that affect the Van der Waals forces:

1. **Number of Electrons Held by the Atom or Molecule:** The strength of Van der Waals forces depends primarily on the number of electrons in the atom or molecule. So, larger atoms and molecules will have greater forces.
2. **Shape of the Molecule:** For isoelectronic molecules, i.e., isomers with the same number of electrons, the factor that determines the strength of the Van der Waals force is the shape of the molecule and the area of surface contact. If the isomer is branched, then the molecules are closely packed. In this case, the Van der Waals forces will be weak.

6.4.5 Van der Waals Forces in Real Life

1. **Gecko:** Van der Waals forces are essential in Gecko. Gecko uses Van der Waals forces to stick on surfaces and climb walls. They have setae on the pads of their feet, allowing them to climb extremely smooth surfaces like glass. This force comes from fluctuations in charge distributions between neighboring molecules. The charge fluctuations are in synchronization, thereby creating an attractive force.
2. **Graphite:** Van der Waals forces bonds the different graphite layers using dispersion forces. Graphite is arranged in several layers of thin sheets. Between each layer, there are Van der Waals intermolecular forces that are weak in comparison to the regular C-C

covalent bonds. For each carbon atom, there is a delocalized electron since carbon only forms three bonds. As all the delocalized electrons move around in the sheet, very large temporary dipoles will induce opposite dipoles in the sheets above and below. Eventually, the induced dipole will be present throughout the whole crystal.

6.4.6 Importance of Van der Waals Forces

Importance and applications of Van der Waals forces are as

- Helps in stabilizing the protein structure.
- Responsible for the stability of the polymer chain.
- Account for the cohesion of inert gases in solid and liquid states.
- Accounts for physical adsorption of molecules to solid surfaces.
- Responsible for adhesion and stability of colloids.

Van der Waals forces provide the necessary interactions that **allow molecules to come together and form stable assemblies without needing strong covalent bonds**. These weak attractions enable the organized arrangement of molecules through processes like stacking or layering.

6.5 APPLICATIONS OF NANOTECHNOLOGY

Nanotechnology applications in development can be broadly divided into several areas: the development of tools that enable the research and ultimately the technology, applications relating to new or improved materials, applications within the sphere of electronics and IT, advances in health and medicine; improvements in cosmetic products and advances in food technology; developments in products for military and security use and space exploration and products and processes to improve the environment. Nano technology has tremendous development in the fields of material science, electronics, biomedical science, biotechnology, military and the environment. The computing and electro communications industries are driving large investments with the aim of maintaining the relentless technological advances that the structure of those industries seems to demand. In Biomedical science, the driving force for innovation is as much political as economic, as spending on medical research seems to be one of the most popular and widely supported forms of public spending in western economies.

- **Material Science:** The science of metals, ceramics, colloids and polymers, has always concerned itself with controlling the structure of materials on the nanoscale. Here, nanoscale science and technology will largely facilitate incremental advances on existing materials and technologies. The improved control over nanoscale structure and better understanding of relationships between structure and properties, will continue the long-run trend towards materials that are stronger and tougher for their weight. Some specific areas in which Nano science technology is contributing to materials science now include: new forms of carbon; nanocomposites; quantum dots and wires and nanostructured materials produced by self-assembly. The cosmetics and paints industries are perhaps perceived as being the most developed in incorporating nanoparticles into their products, for example, the shampoos, skin creams and sunscreens already being used by consumers.

- **Medical:** The medical area of nanoscience application is projected as one of the most potentially valuable, with many projected benefits to humanity. With the advent of new materials and the synergy of nanotechnologies and biotechnologies, it could be possible to create artificial organs and implants that are more akin to the original, through cell growth on artificial scaffolds or biosynthetic coatings that increase biocompatibility and reduce rejection. These could include retinal, cochlear and neural implants, repair of damaged nerve cells and replacements of damaged skin, tissue or bone. The diagnostics and drug delivery is likely to benefit from the development of nanotechnology. With nanoparticles it is possible that drugs may be given better solubility, leading to better absorption.
- **Cosmetics:** Cosmetics and personal products companies have been extremely active in using nanotechnology to improve their existing products and to develop new ones. Cosmetics companies were among the first to get products that were labelled as being nano-enhanced to market. Shampoos and skin creams, containing nanoparticles with the ability to deliver the desired ingredient to where it is needed.
- **Military:** In the field of military, improved materials, lighter but with tough, heat resistant properties, are being used in the design and construction of spacecraft and satellites and this process will gain from nanotechnology. There is also the possibility of nanotechnology facilitating improvements in civilian security equipment. The Institute of Nanotechnology suggests fingerprinting will become cheaper, quicker and more effective using DNA techniques involving nanotechnology and there is also the possibility that nano-based sensors could be used as electronic detectors ('sniffer dogs') for improved airport security. Quantum dots, fluorescent nanoparticles which glow when exposed to ultraviolet light, may be used as tags and labels to prevent theft and counterfeiting and to trace the course of drugs within the body.
- **Biotechnology:** In the field of biotechnology researchers are looking to nanotechnology as the basis of new implants that will replace lost hearing or vision, as new ways of delivering 'smart drugs' to parts of the human body and as ways of carrying 'body repair' cells to areas where tissue has been damaged. As researchers master this new field, revolutionary concepts such as replacement arteries, nanofiber bone reinforcements, powerful microscopes the size of a pen and new diagnostic technologies are becoming more and more probable.
- **Green Technology:** Nanotechnology can be used to prevent, monitor and alleviate a wide range of environmental problems, while significantly reducing cost and improving performance.
- **Hi-Tech:** Nanotechnology provides unprecedented control of light and power. Light emission and/or absorption are crucial for optical communications, display technologies, information storage, solar energy collection, genome sequencing and even targeted drug delivery. The integration of organic/inorganic/mechanical properties can result in self-intelligent systems and self-correcting systems with internal control. Miniaturization is a critical concern for microelectronics, computing and telecommunications industries. Optical routers, large-scale displays and ultra dense molecular memory are only some of the short-term applications.

A cool flat-panel screen will replace your bulky television set at an affordable price, thanks to carbon nanotechnology. This technology will produce better displays at a lower cost, for home theatres, office equipment, portable computing tools and many other applications. Based on a fusion of biology and photonics, there are also potential applications in non-invasive cancer therapies, laser tissue welding, drug delivery and diagnostics.

6.5.1 Lithography and its Types

Lithography is a technique that can be employed to **fabricate materials with specified dimensions and patterns**. Lithography techniques have been widely utilized to create patterned surfaces in microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS). Lithography is a technique used to transfer a two-dimensional pattern onto a flat surface. Depending on the required outcome, many lithography methods can be used.

Types of Lithography:

- Electron Beam Lithography
- Nano Imprint Lithography
- Ion Beam Lithography
- Photo lithography
- X-ray Lithography

1. **Electron Beam Lithography:** Electron beam lithography (e-beam lithography) is a direct writing technique that uses an accelerated beam of electrons to pattern features down to sub – 10 nm on substrates that have been coated with an electron beam sensitive resist. Exposure to the electron beam changes the solubility of the resist, enabling selective removal of either the exposed or non-exposed regions of the resist by immersing it in a developer.

   The primary advantage of electron beam lithography is that it can write custom patterns with sub-10 nm resolution. This form of direct writing has high resolution and low throughput, limiting its usage to photomask fabrication, low-volume production of semiconductor devices and research and development.

   - **Method of Operation:** An Electron beam lithography system uses hardware similar to a scanning electron microscope (SEM) to guide a nanometer sized focused beam of electrons to form a latent image in a layer of resist.

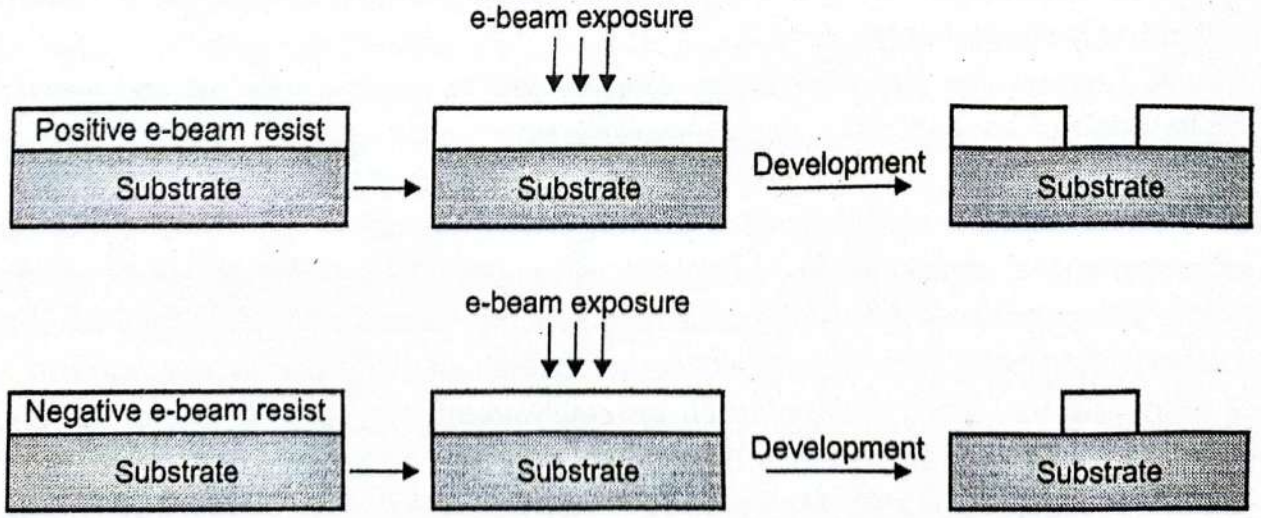


Fig. 6.6: Pattern development using accelerated beam of electrons

The result of this exposure is to render the resist either more soluble (called a positive tone resist) or less soluble (negative tone resist) in an appropriate developer solution. The resulting pattern is then transferred via etching or by depositing other materials. By iterating a number of steps of this type, complex structures of very short length scales can be built up.

Electron beam lithography tools have a certain maximum area that it can write for a fixed stage position know as Write Field. Typically, they range from a few 10s of μms to 1-2 mms. If the pattern to be exposed is more than the size of the write field, the electron beam is blanked, the stage moves by a distance of 1 write field and the writing continues. To avoid discontinuities or overlaps between write fields (known as field stitching errors), an electron beam lithography system has a laser interferometry stage position system that allows stitching of fields with nanometer scale precision.

There is almost always a difference between the digital line width in a pattern and the actual developed feature size after processing. This comes about from electron scattering in the resist. For a well-characterized process, there is generally a fixed difference between the digital size and the actual size, known as bias. This can be implemented by altering all the sizes in the design as appropriate.

Pattern fidelity is limited by electron-matter interactions especially in layouts with a high feature density. The electron scattering within the resist and froms the substrate results in undesired exposures of the resist in regions adjacent to the primary incident beam. This effect is known as the "Proximity Effect" in electron beam lithography. Due to proximity effects, corners in the desired patterns are rounded, gap spacing's and linewidths are modified and certain features may even merge together or disappear completely.

Applications:

Applications of e-beam lithography span a wide range of nanostructured devices including but not limited to electronic devices, opto-electronic devices, quantum structures, metamaterials, transport mechanism studies of semiconductor/superconductor interfaces, microelectro-mechanical systems, optical and photonic devices. E-beam lithography can be also used for mask making and direct writing on non-planar substrates.

2. **Nano Imprint Lithography:** Nanoimprint lithography (NIL) is a nanofabrication technique that enables the creation of intricate patterns and structures on the nanoscale range. It involves the transfer of a patterned template onto a substrate using mechanical pressure and heat. This process allows for the replication of nanoscale features (i.e. features below 10 nm) with high precision and resolution. NIL is simple process, cost-effective and high resolution compared to other nanofabrication methods, as it relies on a reusable template and a simple imprinting apparatus, making it suitable for large-scale manufacturing.

- **Principle or Workflow:** Nanoimprint lithography involves spin-coating of a polymer resist on a substrate and pressing a mold over it, causing the resist to fill the mold. The resin is then cured, and the mold is separated from the substrate to reveal the molds pattern replicated on the resist.

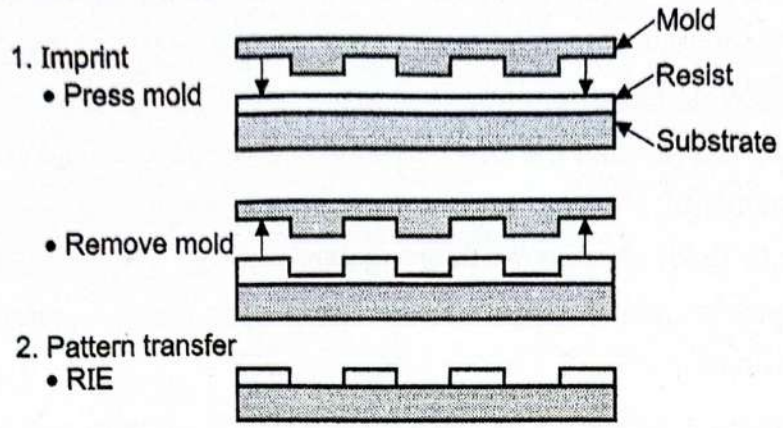


Fig. 6.7: Patterning or workflow using nanoimprint lithography

Nanoimprint lithography have THREE methods that have been developed using different resins and curing methods are as below.

(i) Thermal Nanoimprint Lithography: It uses thermoset or thermoplastic resins cured or melted using a heating cooling cycle. For thermoplastic resins, the heating temperature is kept slightly above the glass transition temperature during pressing. The mold and substrate are separated after cooling. Generally we uses Si, SiO_2/Si, and Ni molds and is highly suitable for compostable and recyclable materials.

(ii) Ultraviolet Nanoimprint Lithography: In this we utilizes UV-curable resins and UV-transmissive mold materials (example: hard quartz and soft polymer molds). After pressing the mold onto a resin-coated substrate, 365 nm UV light is radiated through it. The mold and substrate can be separated immediately without a cooling period. It is used for the rapid, low-cost mass production of nanostructured surfaces due to the resin's low curing time and viscosity

(iii) Soft Nanoimprint Lithography: It including replica molding, micro-transfer molding, and micro contact printing, produce polymeric structures. These techniques rely on surface wetting to pattern substrates using materials in solution form. Soft lithography can form hierarchical microstructures, overhanging features, and 3D architectures from new-generation polymers.

Application:

Nano Imprint lithography offers a range of applications due to its ability to fabricate nanometer scale patterns devices for electrical, optical, photonic and biological applications. *Here are some of the key applications are as below:*

- **Electronics:** NIL is used to fabricate MOSFETs, O-TFTs, and single-electron memory devices, offering a cost-effective method for studying nanoscale device behavior.

- **Optics and Photonics:** NIL is used to fabricate subwavelength resonant grating filters, surface-enhanced Raman spectroscopy (SERS) sensors, polarizers, wave plates, anti-reflective structures, integrated photonics circuits, and plasmonic devices.
- **Opto Electronics:** NIL is used to fabricate LEDs and solar cells.
- **Biomedical:** NIL is used to fabricate micro- and nano-fluidics for biomedical applications, including DNA stretching experiments. It is used to shrink the size of biomolecular sorting device an order of magnitude smaller and more efficient.
- **Materials Science:** NIL is used to process semi-crystalline polymers, improving performance in solar cells, field effect transistors, and ferroelectric memory devices.
- **3D-patterning:** NIL can pattern 3D structures such as damascene interconnects and T-gates in fewer steps than required for conventional lithography.
- **High Aspect Ratio:** NIL can fabricate high-aspect-ratio and hierarchically nanostructured surfaces with limited collapse and defectivity.

6.5.2 Single Electron Transfer (SET)

The manipulation of single electrons was demonstrated in the seminal experiments by Millikan at the very beginning of the 20th century, but in solid state circuits it was not implemented until the late 1980s. The main reason for this delay is that the manipulation requires the reproducible fabrication of very small conducting particles and their accurate positioning against external electrodes.

The necessary nanofabrication techniques have become available during the past three decades and have made possible a new field of solid state physics and electronics. Let a small conductor (traditionally called an island) be initially electro neutral, i.e. have exactly as many (m) electrons as it has protons in its crystal lattice. In this state the island does not generate any appreciable electric field beyond its borders and a weak external force F may bring in an additional electron from outside. (In most single-electron devices, this injection is carried out by tunneling through an energy barrier created by a thin insulating layer).

Now the net charge Q of the island is (-e) and the resulting electric field E repulses the following electrons which might be added. Though the fundamental charge $e \approx 1.6 \times 10^{-19}$ Coulomb is very small on the human scale of things, the field E is inversely proportional to the square of the island size and may become rather strong for nanoscale structures. For example, the field is as large as ~140 kV/cm on the surface of a 10-nm sphere in vacuum.

The theory of single-electron phenomena shows that a more adequate measure of the strength of these effects is not the electric field, but the charging energy,

$$E_C = \frac{e^2}{C} \quad \ldots (1)$$

Where, C is the capacitance of the island.

When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial. In this case the energy scale of the charging effects is given by a more general notion, the electron addition energy E_a. In most cases of interest, E_a may be well approximated by the following simple formula:

$$E_a = E_C + E_k \quad \ldots (2)$$

Here, E_k is the quantum kinetic energy of the added electron,

For a degenerate electron gas,

$$E_k = \frac{1}{g(\varepsilon F)\, V}$$

Where, V is the island volume and g (εF) is density of states on the Fermi surface.

If the island size is reduced below ~10 nm, E_a approaches 100 meV and some single-electron effects become visible at room temperature. However, most suggested digital single-electron devices require even higher values of E_a (~ 100 kBT) in order to avoid thermally-induced random tunneling events, so that for room temperature operation the electron addition energy E_a has to be as large as a few electron volts and the minimum feature size of single-electron devices has to be smaller than ~1 nm.

In this size range the electron quantization energy E_k becomes comparable with or larger than the charging energy E_C for most materials; this is why islands of this small size are called as quantum dots. Their use involves not only extremely difficult nanofabrication technology, but also some major physics problems including the high sensitivity of transport properties to small variations of the quantum dot size and shape. So, it is very important to develop single-electron devices capable of operating with the lowest possible ratio E_a / kBT.

As we know, some devices may work in the size range, Where, $E_C > E_k$ even at room temperature, thus avoiding complications stemming from the energy quantization effects.

6.5.3 Spin Valves

A spin valve is a key component in Spintronic and Data Storage application. Spin valve is a device that exploits the spin-dependent electron transport properties of ferromagnetic materials to control the flow of electrons. It consists of two ferromagnetic layers separated by a thin non-magnetic spacer layer.

A spin valve is a device, consisting of two or more conducting magnetic materials, whose electrical resistance can change between two values depending on the relative alignment of the magnetization in the layers. The resistance change is a result of the giant magnetoresistive effect. The magnetic layers of the device align "up" or "down" depending on an external magnetic field.

In the simplest case, a spin valve consists of a non-magnetic material sandwiched between two ferromagnets, one of which is fixed (pinned) by an antiferromagnet which acts to raise its

magnetic coercivity and behaves as a "hard" layer, while the other is free (unpinned) and behaves as a "soft" layer. Due to the difference in coercivity, the soft layer changes polarity at lower applied magnetic field strength than the hard one.

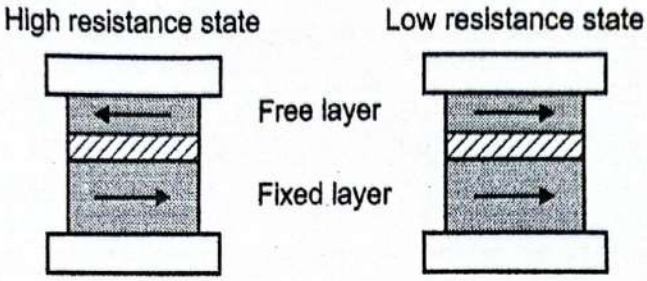


Fig. 6.8: Structure of spin valve

Upon application of a magnetic field of appropriate strength, the soft layer switches polarity, producing two distinct states: a parallel, low-resistance state and an antiparallel, high-resistance state. The resistance of the device depends on the relative orientation of the magnetization in the two ferromagnetic layers, which can be controlled by an external magnetic field. This change in resistance, known as giant magnetoresistance (GMR), forms the basis for various applications in spintronics and data storage.

The Operation of a Spin Valve Relies on Several Key Concepts in Spintronics

- **Spin-Dependent Transport:** In ferromagnetic materials, the electrical conductivity depends on the spin orientation of the electrons. Electrons with spins aligned parallel to the magnetization of the material experience less scattering and have a higher conductivity compared to electrons with antiparallel spins.
- **Giant Magnetoresistance (GMR):** GMR is the large change in resistance observed in a spin valve when the relative orientation of the magnetization in the ferromagnetic layers is switched between parallel and antiparallel states. The resistance is low when the magnetizations are parallel and high when they are antiparallel.
- **Magnetic Anisotropy:** Magnetic anisotropy refers to the preference for the magnetization to align along a particular direction, known as the easy axis. In spin valves, one ferromagnetic layer (the pinned layer) has its magnetization fixed by coupling to an antiferromagnetic layer, while the other ferromagnetic layer (the free layer) can switch its magnetization in response to an external magnetic field.

Structure and Operation of Spin Valves:

A typical spin valve consists of the following layers

- **Pinned Layer:** A ferromagnetic layer with a fixed magnetization direction, usually achieved by coupling to an adjacent antiferromagnetic layer.
- **Spacer Layer:** A thin non-magnetic layer, typically made of copper that separates the pinned and free layers. The thickness of the spacer layer is critical for achieving the desired GMR effect.

- **Free Layer:** A ferromagnetic layer whose magnetization can be switched by an external magnetic field. The orientation of the free layer's magnetization relative to the pinned layer determines the resistance of the spin valve.

The Operation of a Spin Valve can be Understood as Follow

- When the magnetizations of the pinned and free layers are parallel, electrons with spins aligned to the magnetization can pass through both layers easily, resulting in a low resistance state.
- When the magnetizations of the pinned and free layers are antiparallel, electrons with spins aligned to the magnetization of one layer will be scattered in the other layer, leading to a high resistance state.
- By applying an external magnetic field, the magnetization of the free layer can be switched between parallel and antiparallel states, thereby changing the resistance of the spin valve.

Applications of Spin Valves

- Magnetic Field Sensors.
- Magnetic Random Access Memory (MRAM).
- Hard Disk Drive (HDD) Read Heads.

QUESTIONS

1. What is the size range of nanomaterials?
2. Define nanotechnology?
3. Discuss the applications of nanotechnology.
4. What are nanomaterials? Give their classifications?
5. Explain classification of nanomaterials in brief.
6. How are nanomaterials synthesized? Describe any one method.
7. Describe any one method of nanomaterials synthesis.
8. What are the approaches used in synthesis of nanomaterials?
9. Explain any two synthesis methods of nanomaterials preparation.
10. Describe Ball milling method of nanomaterials synthesis.
11. Discuss Sol-gel Method. Give its advantages.
12. What are nanomaterials? What is difference between top-down and bottom-up approach of synthesis?
13. How do the properties of nanomaterials differ from bulk materials?

14. Write the reasons for change in properties of materials at nanoscale.
15. Write short notes on surface to Volume ratio.
16. Define Specific surface area and surface area to volume ratio?
17. Compare specific surface area of cubic nanoparticles of side 100 nm and 5 nm.
18. Compare specific surface area of spherical nanoparticles of size 80 nm and 4 nm.
19. Define Van der Waal forces.
20. Write short note on Van der Waal forces.
21. State importance of Van der Waal forces.
22. Mention the importance of quantum confinement at nanoscale.
23. How are Van der Waals forces and ionic bonds similar?
24. What is meant by Quantum confinement?
25. Explain 0D, 1D, 2D and 3D nanomaterials.
26. Explain the term lithography.
27. State principle of lithography Give its types.
28. What is lithography?
29. Explain the basic steps involved in a typical lithography process.
30. State principle of electron beam lithography and explain its working.
31. Give the applications of Lithography.
32. Explain the term "single electron transfer".
33. Explain the term quantum dots.
34. Explain the term "Single valve".
35. Give the applications of single valves.
36. Explain the structure and operation of single valves.
37. State the applications of Nanomaterials in Engineering or any other fields.
38. Define top-down and bottom-up nanofabrication.
39. Explain briefly the advantages and applications of sol-gel process.
40. Discuss the main properties of nanomaterials.
41. Explain the mechanical properties of nanomaterials.
42. Explain the structural properties of nanomaterials.
43. Explain the optical properties of nanomaterials.
44. Explain the electrical properties of nanomaterials.

45. Write the names of synthesis techniques of nanomaterial.
46. State principle of Nano Imprint Lithography and explain its working.
47. Give any four applications of Nano Imprint lithography.
48. Explain the term: Reactive Ion Etching (RIE) in lithography.
49. What is 3D lithography?
50. Define the term: Sub Wavelength (SW) in lithography.
51. Justify, how Nano Imprint Lithography (NIL) works.

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